REFERENCE MANUAL

LINEAR MIXED-SIGNAL DESIGN SEMINAR

TEXAS INSTRUMENTS

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1995
LINEAR MIXED-SIGNAL DESIGN SEMINAR

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CONTENTS

Introduction

Linear Design Seminar Structure

The 1995 Texas Instruments Linear & Mixed Signal Design Seminar introduces over 40 new products, including devices for battery-powered, low supply voltage and space-restricted applications. We demonstrate how these can be used to address a range of problems and needs experienced by today's design engineers, illustrating the concepts and ideas by tested application circuits.

The sections of the seminar can be related to the simple functional block diagram of a generic electronic system encompassing "linear" (or "real-world") inputs and outputs, whose heart is digital processing.

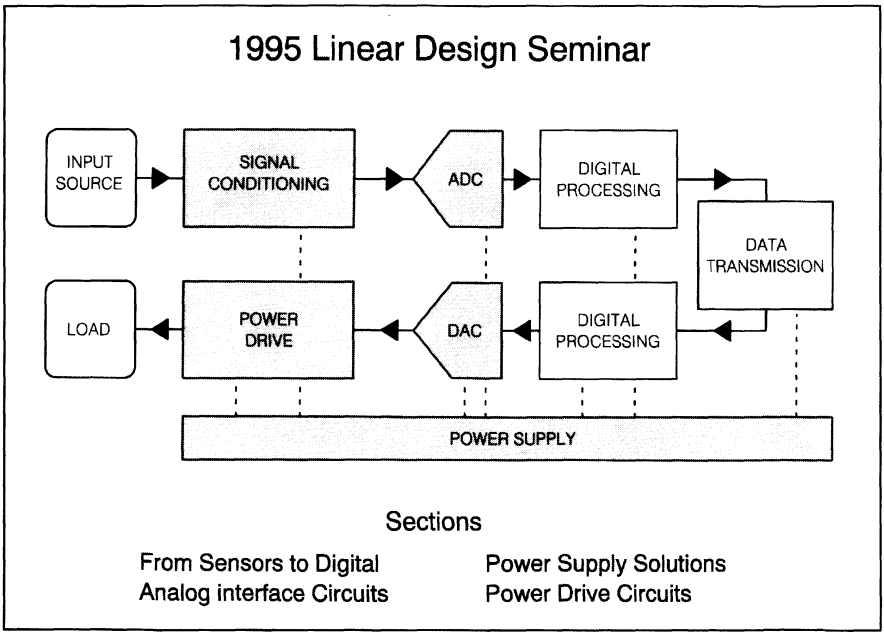

Figure i.1 - 1995 Linear Design Seminar

There are four sections to the seminar:

FROM SENSORS TO DIGITAL
ANALOG INTERFACE CIRCUITS
POWER SUPPLY SOLUTIONS
POWER DRIVE CIRCUITS

In the **SENSORS TO DIGITAL** section we look at the task of converting the analog output of a sensor to a form that can be processed by a digital circuit, for example a microcontroller or a digital signal processor. We consider the choice of signal conditioning components and their use with analog-to-digital converters.

First there is discussion of the special needs of 3 volt systems which is illustrated by a precision 3v pressure sensor measurement. Next some recent 5v converters are described, and illustrated by applications in motion control.

Lastly some recent opto sensors which simplify the task of light measurement are examined.

In the **ANALOG INTERFACE CIRCUIT** section we consider recent product introductions where the task of bridging the gap between the 'real' analog world and the digital processor has been realised by specific integrated components. These are particularly important where space and cost are of great importance, and the generic application uses large volumes of product, to lower the specific development costs.

Analog interface components may contain signal conditioning (amplification, buffering, filtering) and conversion elements as well as appropriate interfaces to digital processing systems.

An important concern is the simplicity of interface between these analog interface components and the digital part of the system.

Topics covered will be "voice-based audio processors", relatively low-cost integrated components operating up to 3-5 volts; audio interface circuits with high performance and programmability from DSP; audio data converters; and lastly Video Interface Palettes that deliver the large amount of visual information stored in memory to colour PC monitors.

In the section on **POWER SUPPLY SOLUTIONS** we are concerned with delivering a stable supply to our analog and digital circuits and of ways to preserve the integrity of both information and indeed the digital processor under out-of-specification external conditions (eg start-up, over-voltage, etc).

Lastly in **POWER DRIVE SOLUTIONS** we consider new integrated power switches that employ the small component feature size developed for today's high speed digital processors and high density memories.

In this section we are concerned with applications where significant power is dissipated, and practical drive circuits for motors, lamp arrays and relays are described.

Section 1
From Sensors to Digital

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TEXAS INSTRUMENTS

Contents Section 1

1 Introduction

This section looks at some typical sensor to digital applications and uses them to illustrate how sub-system components can meet the needs of today's designers.

1.1 Sub-System Components

The appetite for totally integrated solutions to applications problems is undoubtedly growing. As soon as the demand for a particular function or set of functions has increased to an economically viable level, it would seem that an integrated circuit is designed to meet the need.

However the age of the ubiquitous operational amplifier or the slightly more esoteric data converter is far from over. It is the nature of electronics that its applications are widely dispersed across every facet of human activity. This fact should safeguard the future of the sub-system component for several more years yet !

It is the task of the system designer to decide what level of integration is appropriate for the particular application problem he is attempting to solve. His decision will be influenced by performance needs and cost constraints. Moreover, the higher performance available with many standard sub-system components ensures that they will frequently be preferred to more integrated solutions.

1.2 Mixed Signals

Solutions to real world problems require an ability to handle analog and digital signals equally efficiently. The need to get analog information into the digital domain accurately and rapidly is more important today than ever before. Despite the proliferation of microcontrollers and digital signal processors which now include analog functions on board, the demand for individual components which offer higher performance continues to grow. This first section will attempt to show why this is the case.

1.3 Sensors to Digital

The key elements of a typical electronic sensor system are shown in figure 1.1. The transducer provides a convenient analogy of the physical phenomenon to be measured. This analogy may be in any one of a number of forms including current, voltage. resistance or capacitance for example.

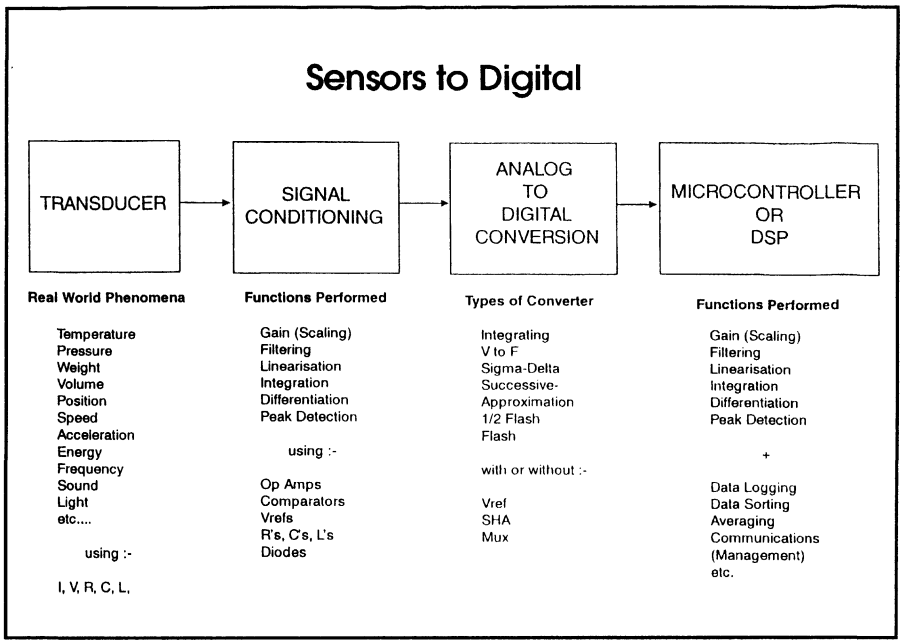

Figure 1.1 - Key Elements of a Sensor-to-Digital System

It is the role of the signal conditioning to modify the form of the signal to make it convenient for the analog-to-digital converter (ADC) to handle and produce an accurate conversion. Gain, filtering, linearisation, integration and differentiation are examples of the transfer functions which can be applied to the signal in order to provide the ADC with a useful analog input. The most common active component found in signal conditioning stages is the operational amplifier.

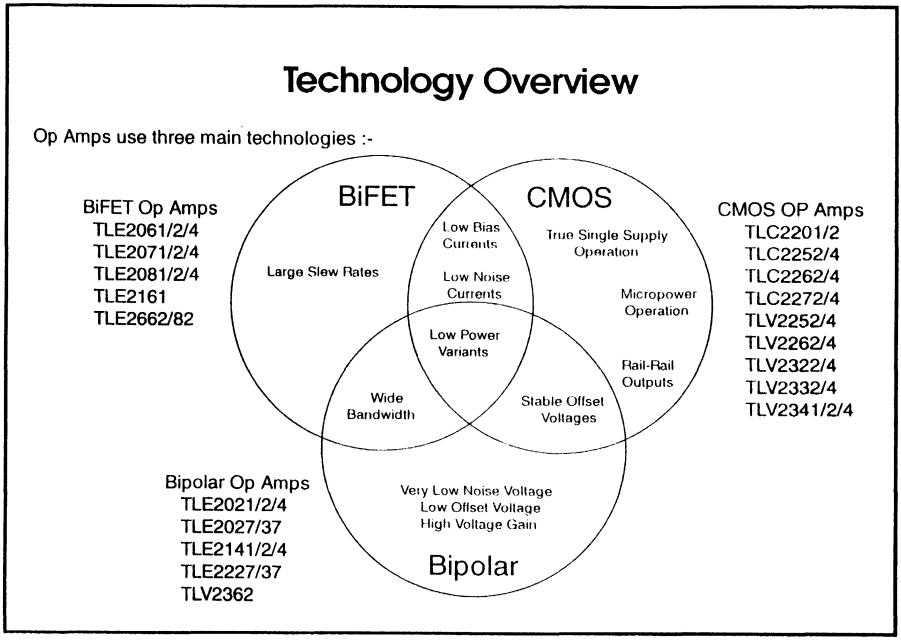

Figure 1.2 - Op Amp Technology Overview

Figure 1.2 shows the three main technologies which are used to fabricate op amps. The bipolar process was the first to be used to manufacture monolithic op amps. The basic process has undergone some refinements since the early 1960s. For example transistors have got faster (higher f_t) and process noise levels have improved. However the bipolar process has now been used very effectively for in excess of two decades and is still the most effective process for a number of op amp types. It offers a mix of low noise, wide bandwidth and high gain. The BiFET process includes JFET transistors with the standard bipolar process. This offers the benefit of higher input impedances and lower bias currents.

CMOS offers several useful features including low power consumption, single supply operation and rail-to-rail outputs.

2 3-Volt Supply Considerations

2.1 Technology Trends

Much of the world's electronic systems presently operate off 5-Volt supplies. This is because of the significant historic influence of logic families such as 74 series TTL which run off 5 volts and their large usage by the computer industry.

The growing demand for more features and performance in portable electronic equipment has forced manufacturers of integrated circuits to produce whole new families of devices to meet the need. The common feature of these devices is that they will operate for a longer period of time from the same amount of battery power. Alternatively they will operate for the same amount of time from a smaller battery. Both results offer attractive benefits to manufacturers of portable equipment. There are various ways of achieving this capability.

The most popular method amongst IC manufacturers is to reduce the operating voltage of the devices. This has the effect of reducing the power consumption in direct proportion to the reduction in supply voltage. To maximise the benefit to end users (and thus their adoption) of the new IC product families a concensus was needed on the choice of lower supply voltage. 3 volts has been chosen as offering a sufficiently high saving in power without compromising the performance of the products too much. It is also compatible with popular low voltage battery cells.

3.3-Volt Supply Logic Families

LOGIC FAMILY	ICC (μA)	PROCESS type/microns	EQUIVALENT PERFORMANCE LOGIC FAMILY @ 5-V SUPPLY
* SN74LV	20	CMOS/2.0	HCMOS
* SN74LVC	20	CMOS/0.8	FACT, ACL, F
* SN74ALVC	20	CMOS/0.6	FCT...E Series (IDT)
* SN74LVT	2000	BiCMOS/0.8	ABT

* OPERATING SUPPLY VOLTAGE RANGE : 2.7 - 3.6 Volts

Figure 1.3 - 3.3-Volt Supply Logic Families

2.2 3.3-Volt Supply Logic Families

The trend towards designing systems using 3-volt supplies has been boosted by the availability of new logic families such as those shown in figure 1.3 which operate off 3 volts. As is indicated, the performance of these new families is equivalent to that of existing 5-Volt series devices. Other benefits accrue from using 3-Volt supplies besides power consumption. Noise generated by current spikes is reduced significantly from those occuring with 5-Volt supplies.

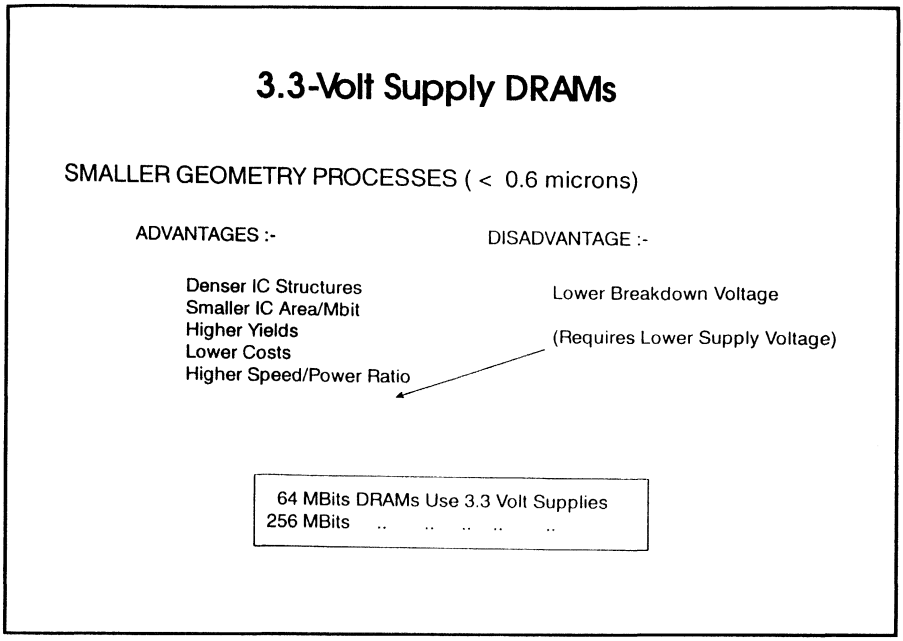

Figure 1.4 - 3.3-Volt Supply DRAMS

2.3 3.3-Volt Supply DRAMs

The trend towards memories operating off lower supply voltages has been driven as much by technological expediency as by customer demand. To achieve higher memory capacity denser IC processes have been required. These utilise smaller minimum device geometries which, in turn, can withstand lower breakdown voltages. Furthermore the problem of power dissipation becomes significant when dealing with 64-Mbit DRAMs or larger memories. One way to alleviate the problem is to reduce the supply voltage. The speed/power ratio of each memory cell is increased significantly for memories designed to operate off a 3.3-Volt supply.

The availability of 64-Mbit DRAMS operating off 3.3-Volt supplies is further enhancing the demand by end-equipment manufacturers for other supply compatible ICs. Amongst these are linear components such as operational amplifiers and analog-to-digital converters.

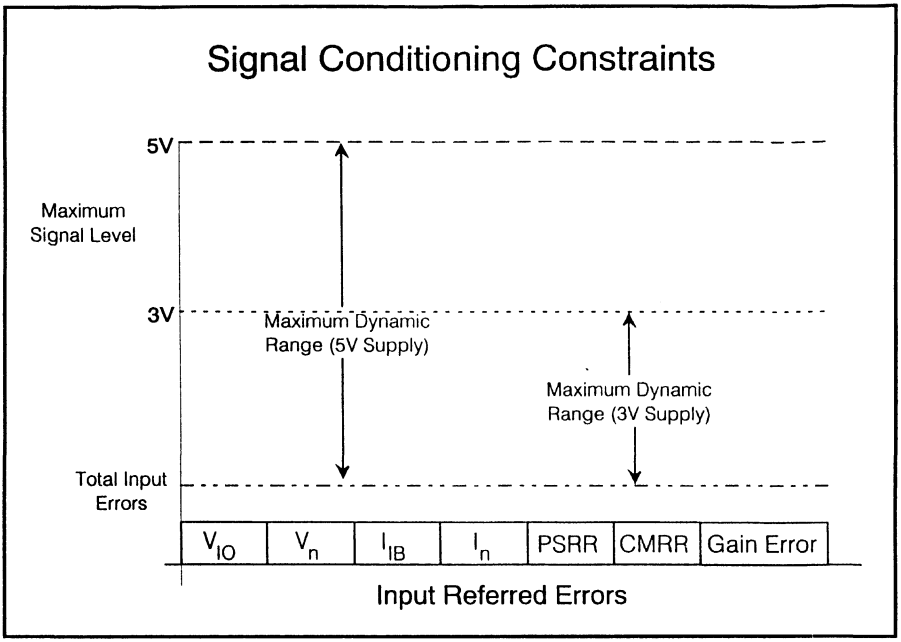

Figure 1.5 - Signal Conditioning Constraints

2.4 Signal Conditioning Constraints

The high noise immunity of digital signals is one of its great advantages over analog signals. This fact helps to prevent the performance of logic families and DRAMS from being greatly affected by a reduction in supply voltage to 3.3 volts.

However, devices such as op amps and ADCs which contain linear functions are much more susceptible to the effects of noise. A reduction in their supply voltage will reduce the dynamic range of the signals which they can handle and will ultimately limit the performance which they can achieve. Figure 1.5 illustrates how the dynamic range of a typical linear component will be reduced by operating the device off a 3-Volt supply instead of 5 volts. This caused simply by the reduction in maximum signal swing which is possible at 3 volts.

It is important, therefore, that as much of the reduced supply range as possible is available for useful signal swing. This is achieved by using products such as rail-to-rail output operational amplifiers.

Advanced LinCMOS™
Rail-to-Rail Output Op Amps

DEVICE	SUPPLY (V) (Rated)	SUPPLY (V) (Min)	VOH (Min) IOUT = 20 μA	VIO (max) mV	GBW (MHz)	Dual / Quad
TLC2252	+5	4.4	4.98	1.5	0.2	Dual
TLC2254	+5	4.4	4.98	1.5	0.2	Quad
TLC2262	+5	4.4	4.99	1.5	0.8	Dual
TLC2264	+5	4.4	4.99	1.5	0.8	Quad
TLC2272	+5	4.4	4.99	1.5	2.1	Dual
TLC2274	+5	4.4	4.99	1.5	2.1	Quad
TLV2252	+3	2.7	2.98	1.5	0.18	Dual
TLV2254	+3	2.7	2.98	1.5	0.18	Quad
TLV2262	+3	2.7	2.99	1.5	0.7	Dual
TLV2264	+3	2.7	2.99	1.5	0.7	Quad

Figure 1.6 - Advanced LinCMOS™ Rail-to-Rail Output Op Amps

Texas Instruments manufactures a growing number of rail-to-rail output operational amplifiers, illustrated in figure 1.6, some of which are specified to operate off 3.3-volt supplies. Note that the performance of these low voltage devices is specified at a single 3.3-Volt supply. However they will operate with a supply voltage of between 2.7 volts and 3.6 volts.

3 3-Volt Supply Sensor Systems

3.1 Introduction

Powering transducer electronics off 3-Volt supplies is beneficial in a number of significant applications ranging from portable parametric test equipment to remote telemetry systems. However it is desirable to match the performance of the sensor with that of the sensor-to-digital electronics. This can be a challenge when operating the system off only 3 volts. This sub-section of the seminar looks in particular at pressure sensors, their applications and how to implement a portable pressure sensing system running off a single 3-Volt supply.

3.2 Pressure Sensor Applications

Pressure Sensor Applications

APPLICATION	RESOLUTION (bits)
Automotive	6-7
Industrial Control	8-10
Pressurised Telephone Lines	8-10
Gas Pipe Line Monitors	8-10
Portable Pressure Meters	8-12
Medical Equipment	8-16
Meteorology	12-16

Figure 1.7 - Pressure Sensor Applications

As can be seen in figure 1.7 pressure sensors are used in a wide range of applications requiring various resolutions between 6 and 16 bits. Industrial applications such as process control and portable pressure meters often require 8 to 10 bits of resolution with up to 9 bits of absolute accuracy.

The most popular type of pressure sensor is the silicon variety which is used in many of the applications mentioned in figure 1.7.

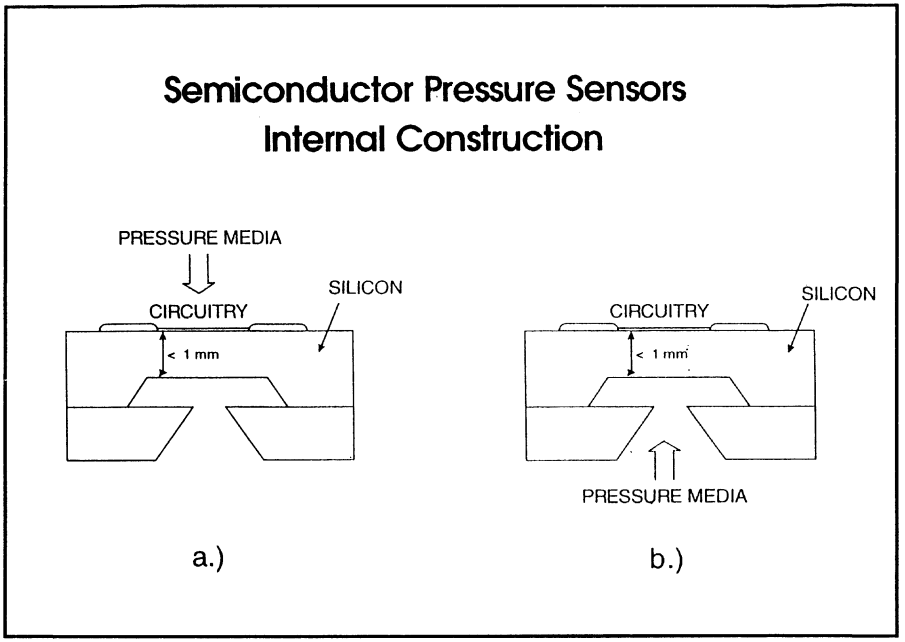

Figure 1.8 - Semiconductor Pressure Sensors - Internal Construction

Figure 1.8 shows a cross section of the internal construction of a silicon type pressure sensor. The pressure transducer is formed by a resistive bridge which is fabricated on the top surface of a piece of silicon. The resistors may be thin film or diffused types. The underside is etched or micro-machined to form a thin layer of silicon beneath the bridge. This layer, which is frequently less than 1 mm thick, is deformed slightly when subjected to a change in pressure. This causes a change in the stress pattern on the silicon surface which in turn causes a change in the relative resistance of the arms of the bridge. This produces a change in the output voltage of the bridge. To increase the sensitivity of the sensor the layer of silicon underneath the bridge is made thinner.

The IC is then mounted on a second piece of silicon. This supports the bridge assembly and allows metal fixings and couplings to be attached. It also helps to absorb stress which may be caused by differences in coefficients of thermal expansion between the metal couplings and the silicon.

When in use, the sensor can be deployed with the upper surface in contact with the fluid or gas to be measured. This has the disadvantage that the bridge circuitry and its metal contacts can be adversely affected by various substances in the pressure medium.

Alternatively the gas or fluid can be in contact with the underside of the IC. This avoids contamination of the bridge by elements in the pressure medium. The bridge will now be deformed in the opposite direction so the output from the bridge will be in the reverse sense of that produced by pressure acting on the upper surface.

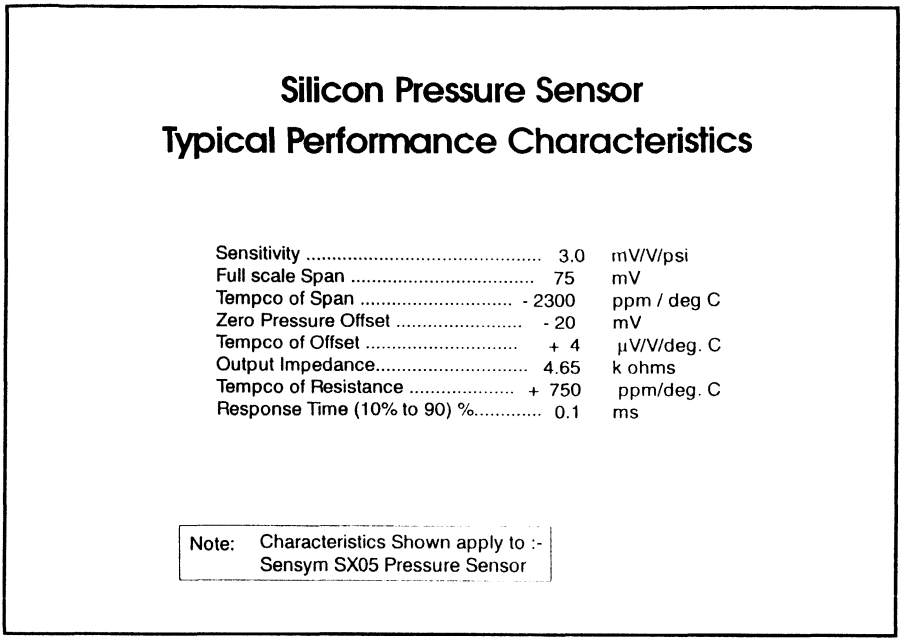

Figure 1.9 - Silicon Pressure Sensor - Typical Performance Characteristics

The typical performance characteristics of a silicon pressure sensor (Sensym SX05) are shown in figure 1.9. It can be seen that the effects of temperature on span and offset is significant. It is therefore necessary to calibrate the pressure measurement system electronics to compensate for these effects.

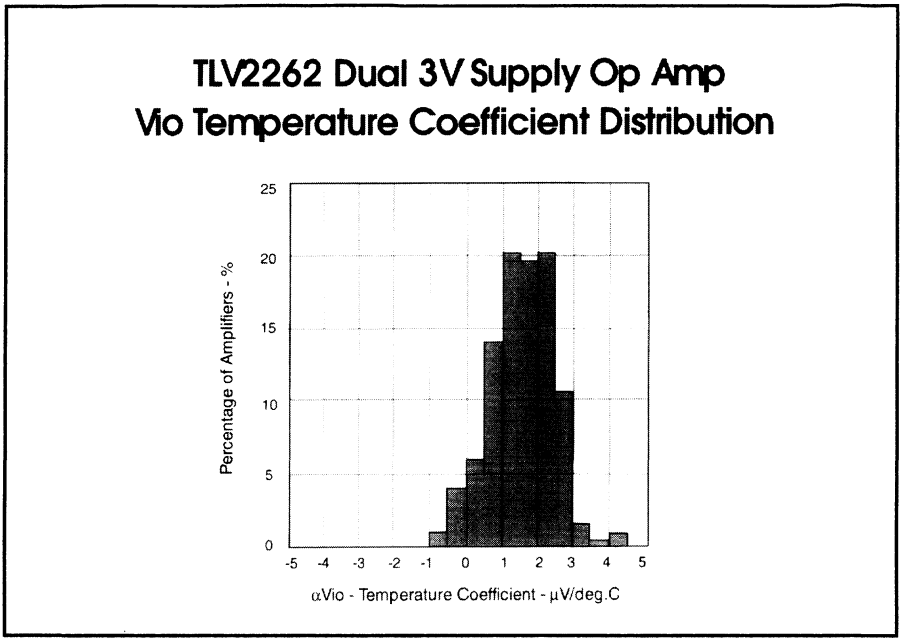

Figure 1.10 - TLV2262 Vio Temperature Coefficient Distribution

The size of the offset of the pressure sensor is large compared to the input offset voltage (Vio) of non-precision operational amplifiers such as the TLV2262. Furthermore the temperature coefficient of Vio of the TLV2262 is typically less than 4 μV/°C, as shown in the histogram of figure 1.10, which is one third of the offset temperature coefficient of the pressure sensor when excited by a +3-Volt power supply. This is because the temperature coefficient of offset of the pressure sensor is 4 μV per volt of excitation per degree Centigrade which equates to 12 μV/ °C for 3-Volt supply.

It is therefore attractive to compensate for the offset and offset temperature coefficients of both pressure sensor and operational amplifier at the same time.

TLV2262 3-V Supply Dual Op Amp

Features

Input Offset Voltage VIO	0.3 V (typ) 2.5V (max)
Input Offset Voltage Tempco	2 μV/°C (typ)
Input Bias Current	1 pA (typ) 150 pA (max)
High Level Output Voltage (Iout - 100 μA)	2.85 V (min)
Low Level Output Voltage (Iout - 500 μA)	0.15 V (max)
Supply Current - IDD	500 μA (max)
Input Noise Voltage	43 nV/√Hz (typ) @ f = 10 Hz 12 nV/√Hz (typ) @ f = 1 kHz
Input Noise Current	0.6 fA/√Hz (typ)
Gain-Bandwidth Product	670 kHz (typ)

Figure 1.11 - TLV2262 3-Volt Supply Dual Op Amp

The TLV2262 offers several features which are attractive in portable pressure sensor applications. Some of these features are shown in figure 1.11. They include rail-to-rail output signal swing with useful output currents in excess of 100 μA available across the output voltage range.

The typical input noise voltage of the TLV2262 at 10 Hz is 43 nV/√ Hz. Over 100 Hz bandwidth this produces an average effect of less than 1 μVrms which is a small fraction of a least significant bit (LSB) at 10-bits of resolution.

The typical input noise current of the TLV2262 is 0.6 fA/√ Hz. This yields relatively insignificant noise voltages even when flowing through circuit impedances of the order of 1 MΩ !

TLV1543 3.3-Volt Supply 10-bit Serial ADC

Features

- 3.3 Volt Supply Operation
- On-chip sample-hold
- Serial Data Output
- SPI Compatible
- 10-bit Resolution (+ /- 1 LSB TUE)
- 11 Analog Input Channels
- Three built-in Self Test Modes
- On-chip System Clock
- End of Conversion (EOC) Output
- 21 µS Conversion Time

Figure 1.12 - TLV1543 3.3-Volt Supply 10-bit Serial ADC

The TLV1543 is a 10-bit serial data output analog-to-digital converter which operates with a 3-Volt supply. Its multiple-input-channel architecture makes it particularly suitable for use in auto calibrated sensing applications. One input channel can be used to convert the amplified sensor signal while another channel can convert a temperature signal.

Both the TLV2262 operational amplifier and the TLV1543 10-bit ADC are used in the calibrated pressure sensor system design which follows.

3.3 A Fully Calibrated Pressure Measuring System

3.3.1 System Overview

This application demonstrates how a fully calibrated portable pressure measuring system running off a single +3-V supply can be built. The system offers 10-bit resolution and 9-bit accuracy.

The pressure sensor (type: Sensym SX05) which was used is based on the piezoresistive effect. It consists of four silicon resistors, which are electrically connected to form a Wheatstone bridge. The excitation voltage is connected across one of the two diagonal junctions of the bridge. The pressure signal is extracted as the differential voltage between the other two diagonals. This signal is amplified by a differential amplifier which consists of the TLV2262 and four resistors as shown in figure 1.13.

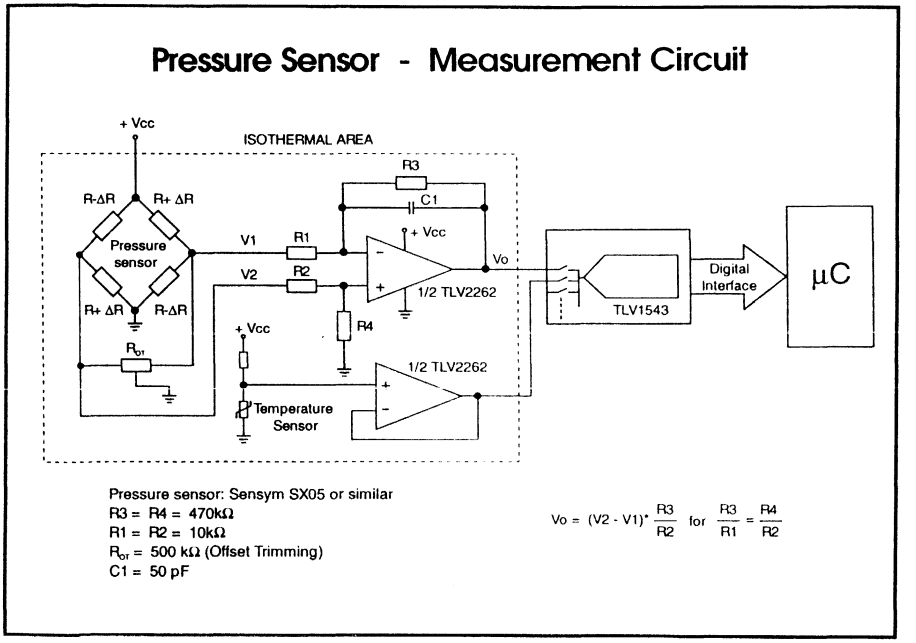

Figure 1.13 - Pressure Sensor - Measurement Circuit

The gain of the amplifier is chosen to scale the signal so that the output voltage of the operational amplifier, and thus the input to the following ADC, is around 2.5 Volts, at maximum input pressure for the SX05 type sensor. The measuring system runs off a single 3-V supply. To compensate for negative pressure transducer offsets it is necessary to connect a trimming potentiometer, P1, across the output of the sensor with the wiper routed directly to the negative rail as shown in figure 1.13. The ouput signal of the operational amplifier is directly connected to the TLV1543 10-bit serial output ADC. The operation of the ADC is controlled by a microcontroller. The measuring scheme was

implemented first using the TMS7000 microcontroller followed by the M68B11. These were chosen because they both operate from a 3-V single supply.

3.3.2 Derivation of System Formula

The system exhibits two significant error effects which must be compensated for each time a pressure measurement is made. These errors, which vary with temperature, are system offset and system gain (otherwise known as slope). The pressure sensor and amplifier combination is treated as a "black box". This has two advantages. It simplifies the necessary calibration routine and also allows the offsets and gain errors of a non-precision amplifier to be lumped in with those of the pressure sensor.

The total circuit yields a family of temperature dependent linear characteristics as shown in figure 1.14.

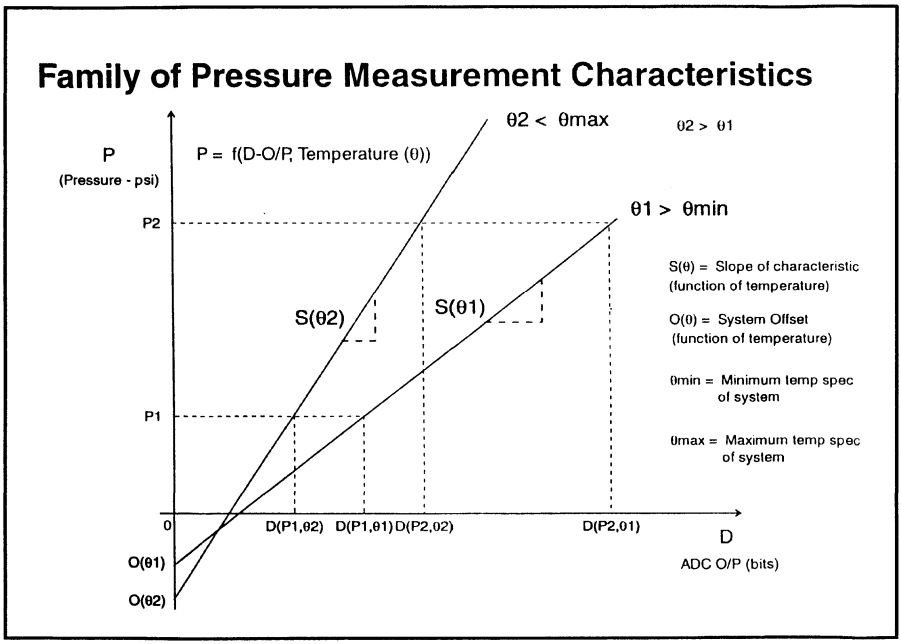

Figure 1.14 - Family of Pressure Measurement Charateristics

Derivation of the system-formula:

Function of the linear characteristic: $P = D^* S(\theta) + O(\theta)$ [1]

Slope as a function of the temperature: $S(\theta) = S(0°C) + \theta_A * TK_S$ [2]

Offset as a function of the temperature: $O(\theta) = O(0°C) + \theta_A * TK_O$ [3]

with θ_A = ambient temperature

Therefore:

System formula: $P = D^*(S(0°C) + \theta_A * TK_S) + O(0°C) + \theta_A * TK_O$ [4]

TK_S - Tempco of Slope

TK_O - Tempco of Offset

Figure 1.15 - Derivation of the system formula

The circuit shown in figure 1.13 allows the system offset and gain errors to be automatically compensated for. The effects of offset and gain changes due to temperature on the pressure measurement can be described by the following system formula :-

$$P = D\,((S(0°C) + \theta_A\ TK_S) + O(0°C) + \theta_A\ TK_O$$

where :-

P	=	Actual Pressure (psi)
D	=	ADC Output
O(0°C)	=	Offset of system at 0°C
O(θ)	=	Offset of system at θ°C
S(0°)	=	Slope of system at 0°C
S(θ)	=	Slope of system at θ°C
θ_A	=	Ambient Temperature
TK_O	=	System Offset Temperature Coefficient
TK_S	=	System Slope Temperature Coefficient

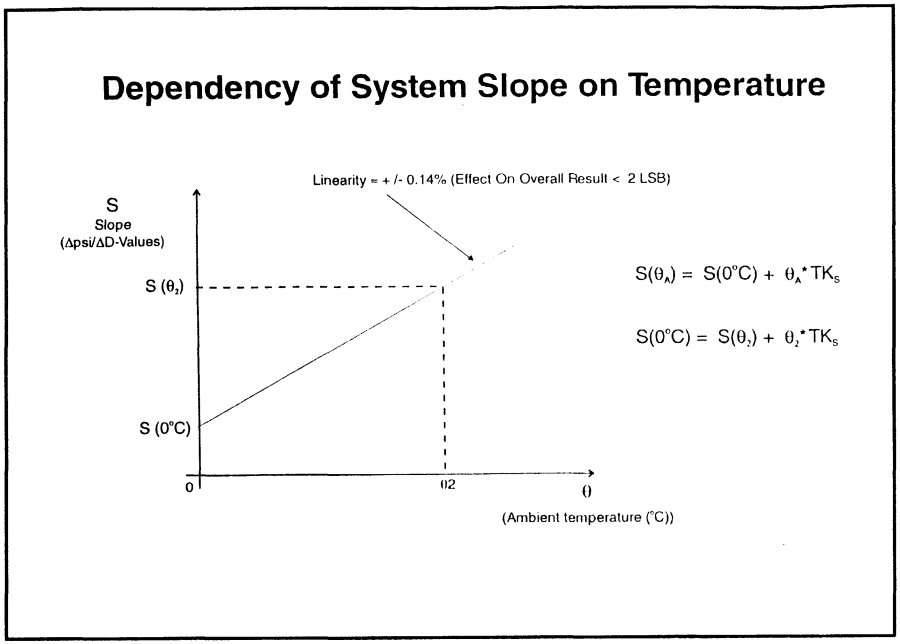

Figure 1.16 - Dependency of Slope (Gain) on Temperature

This system fomula is derived by substituting equations 2) and 3) in equation 1). Other calibration formulae are shown in equations 5) through 12).

3.3.3 System Calibration

The slope and offset temperature coefficients of the system were measured during the installation. Accurate and stable pressure and temperature measuring equipment is required to perform this task. Several points on the P (pressure) versus D (ADC output) function were measured at a fixed temperature to prove the linearity of the function. These temperature coefficients were then used by the microcontroller in conjunction with the measured pressure and temperature to calculate the true pressure in psi using the system formula.

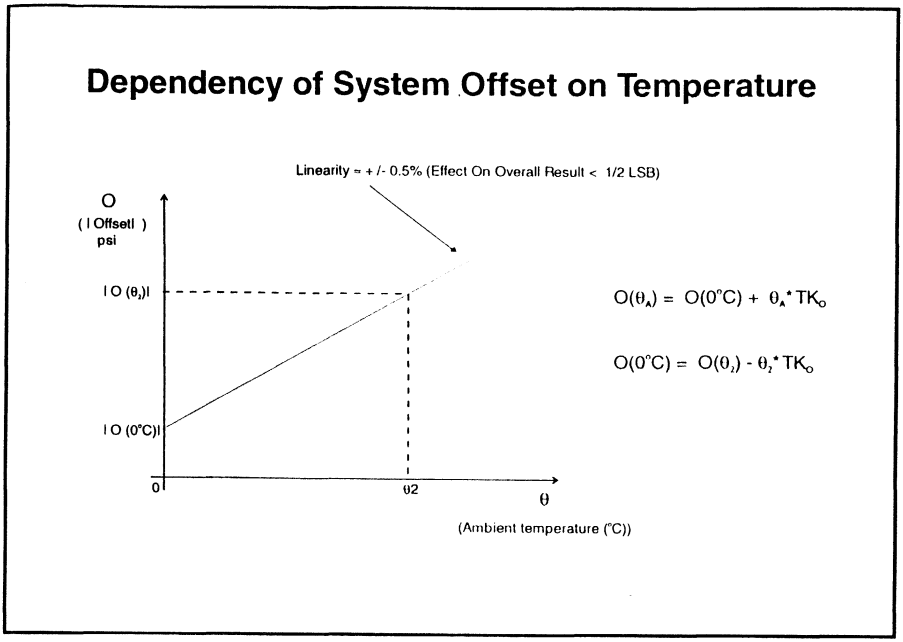

Figure 1.17 - Dependency of Offset on Temperature

Figure 1.17 shows the dependency of the offset of the system on temperature. Measurements indicated that the dependency was quite linear.

Calibration Formulas

Slope, S(θ1), of the characteristic, P = f(D-Value,θ1):

$$S(\theta 1) = \frac{P2 - P1}{D(P2,\theta 1) - D(P1,\theta 1)} \quad [5]$$

Slope, S(θ2), of the characteristic, P = f(D-Value,θ2):

$$S(\theta 2) = \frac{P2 - P1}{D(P2,\theta 2) - D(P1,\theta 2)} \quad [6]$$

Temperature-coefficient, TK_S, of the slope:

$$TK_S = \frac{S(\theta 2) - S(\theta 1)}{\theta 2 - \theta 1} \quad [7]$$

Slope, S, at 0°C :

$$S(0°C) = S(\theta 2) - TK_S \quad [8]$$

Figure 1.18 - Calibration Formulas

The temperature coefficient of the slope (or system gain) is derived using calibration formulas 5) through 8) shown in figure 1.18.

Calibration Formulas

Offset, O(θ1), of the characteristic, P = f(D-Value,θ1):	$O(\theta 1) = P2 - D(P2,\theta 1)^* S(\theta 1)$	[9]
Offset, O(θ2), of the characteristic, P = f(D-Value,θ2):	$O(\theta 2) = P2 - D(P2,\theta 2)^* S(\theta 2)$	[10]
Temperature-coefficient, TK_O, of the offset:	$TK_O = \frac{O(\theta 2) - O(\theta 1)}{\theta 2 - \theta 1}$	[11]
Offset, O, at 0°C:	$O(0°C) = O(\theta 2) - TK_O$	[12]

Figure 1.19 - Calibration Formulas (continued)

The temperature coefficient of the system offset is derived using the calibration formulas 9) through 12) shown in figure 1.19.

The temperature coefficients of offset and slope are then used in the system formula to calculate the actual pressure acting on the sensor.

3.3.4 Temperature Sensor Linearisation

The circuit for temperature measurement is shown in figure 1.20. It consists of a series connected silicon-planar temperature sensor and linearisation resistor. The value of the linearisation resistor, R_L, can be derived with the following equation :-

$$R_L = \frac{R_M (R_1 + R_2) - 2 R_1 R_2}{R_1 + R_2 - 2 R_M}$$

where R_1 = sensor resistance value at minimum temperature point

R_2 = sensor resistance value at maximum temperature point

R_M = sensor resistance at midpoint of temperature span

The signal which is taken from the temperature sensor is buffered by the other half of the TLV2262 dual operational amplifier prior to applying it to one of the other unused input channels of the ADC.

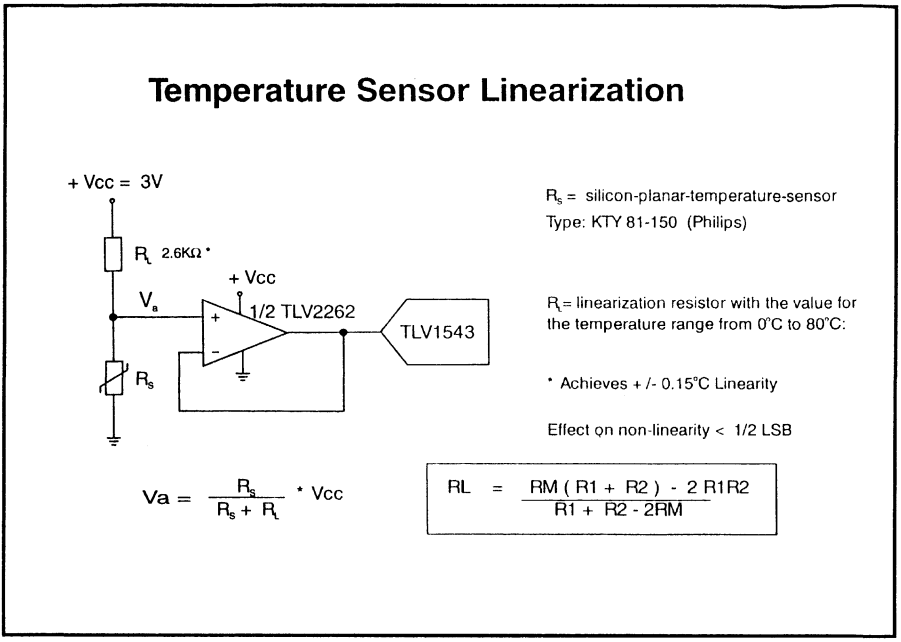

Figure 1.20 - Temperature Sensor Linearisation

The linearisation resistor achieves a linearity of +/- 0.15°C. This is well within the error band needed to calibrate the system to 10-bit resolution.

The sensor interface system was designed to interface to two microcontroller architectures. The TMS7000 and the MC68B11 were chosen because they both operate with a 3-Volt supply.

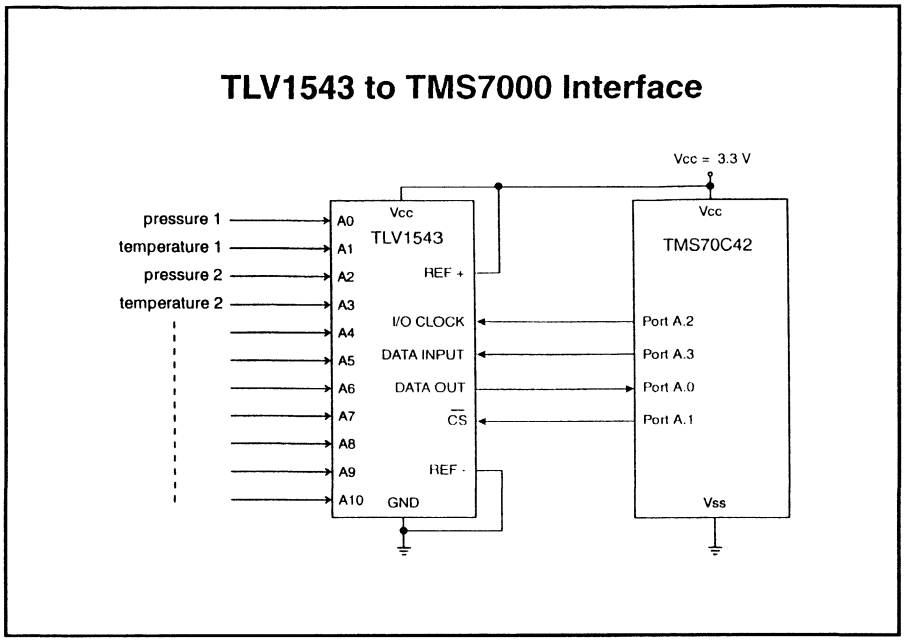

Figure 1.21 - TLV1543 to TMS7000 Interface

The TMS70C42 version of the TMS7000 family of microcontrollers was interfaced to the TLV1543 10-bit ADC using the first four bits of Port A I/O port as shown in figure 1.21.

ADC channel selection data is sent serially to the ADC via Port A.3 (bit3 of Port A). Conversion results are received, via another serial link from the ADC, at Port A.0 of the microcontroller.

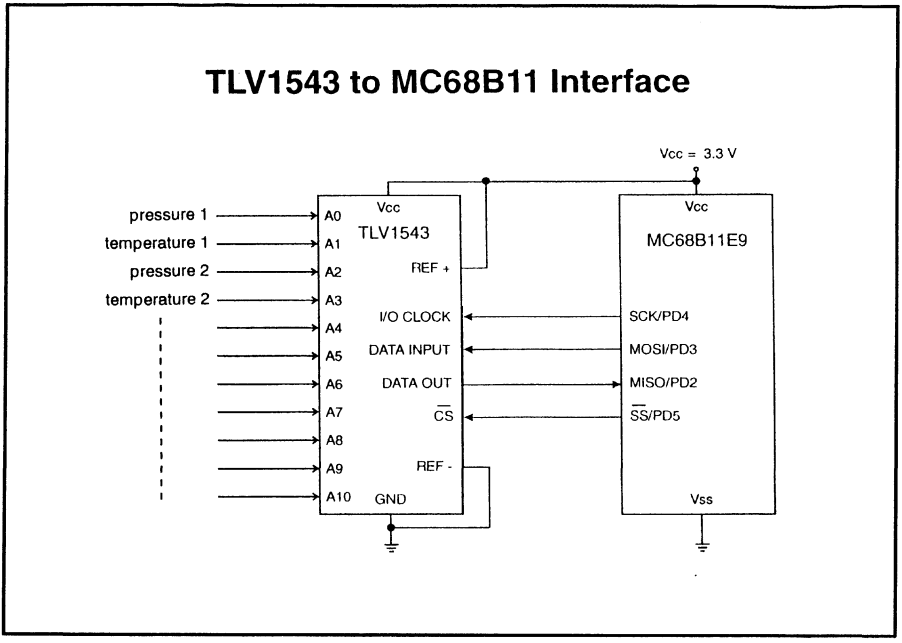

Figure 1.22 - TLV1543 to MC68B11 Interface

Figure 1.22 illustrates the interface of the TLV1543 to the MC68HC11 microcontroller. This uses the Serial Peripheral Interface (SPI) of the microcontroller to transmit and receive serial data to and from the ADC.

4 5-Volt Supply Sensor Systems

4.1 Introduction

The most popular power supply level in present electronic systems is 5 volts. this is largely influenced by the fact that the broadest available range of digital functions operates from a single 5-Volt supply. In the past, many analog functions such as operational amplifiers and ADCs have been designed to operate off +/- 15-Volt supplies. Recently , however, the majority of new linear ICs have been designed to operate from a single +5-Volt supply or dual +/- 5-volt supplies. The performance of these new designs has equalled and in many cases surpassed that of the older +/ 15-Volt supply products.

We now look at how these products are influencing the design of 5-Volt supply sensor systems.

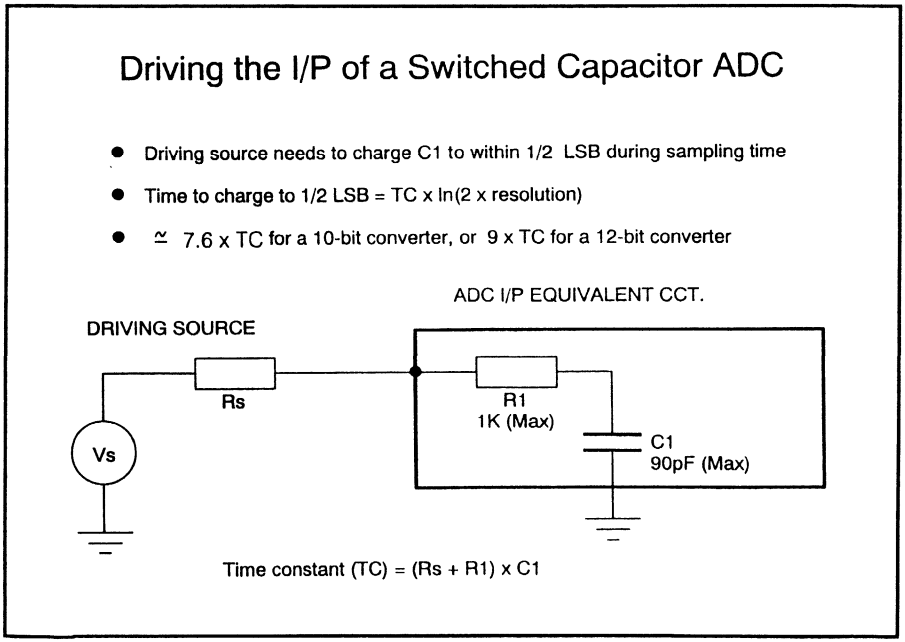

Figure 1.23 - Driving the Input of a Switched Capacitor ADC

4.2 Switched Capacitor ADCs

The versatility and low power consumption of switched capacitor type successive approiximation ADCs make them suitable for a wide range of 5-volt supply sensor interface applications. It is important to take care when driving the analog input to these ADCs to ensure that the source impedance is low enough to be able to charge the input capacitance of the ADC to within 1/2 LSB of the final input value during the sampling time available. Figure 1.23 indicates that the time taken to charge the sampling capacitor to within 1/2 LSB of the analog input voltage level is 9x(TC) where TC is the time constant of the combination of the source resistance in series with the ADCinput resistance and the input sampling capacitor of the ADC.

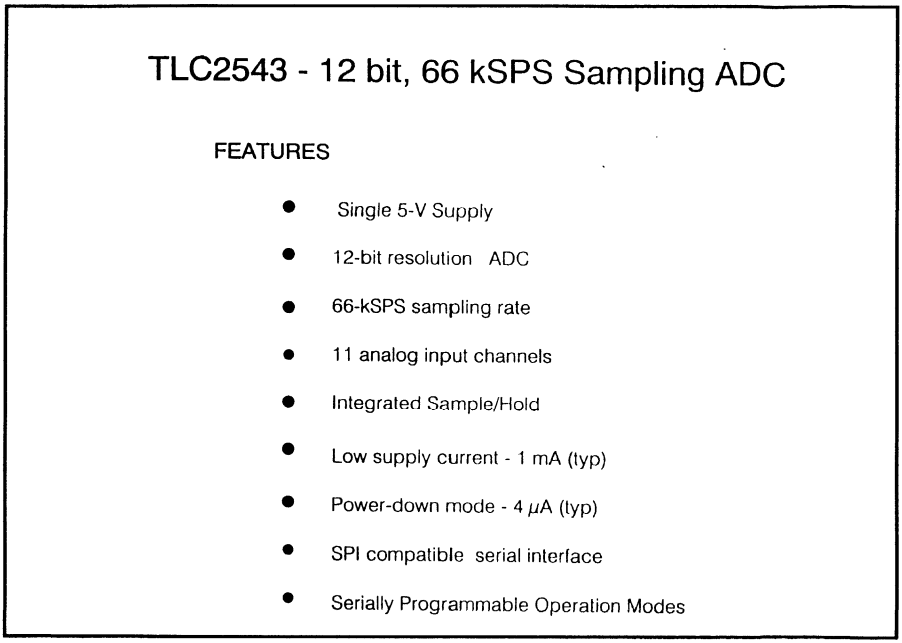

Figure 1.24 - TLC2543 - 12-bit, 66-kSPS Sampling ADC

The TLC2543 is an example of a 12-bit resolution switched capacitor, successive approximation ADC which operates off a single +5-Volt supply. The principal features of the TLC2543 are shown in figure 1.24. The low operating current (1 mA) and power-down facility make this ADC suitable for portable sensor interface systems.

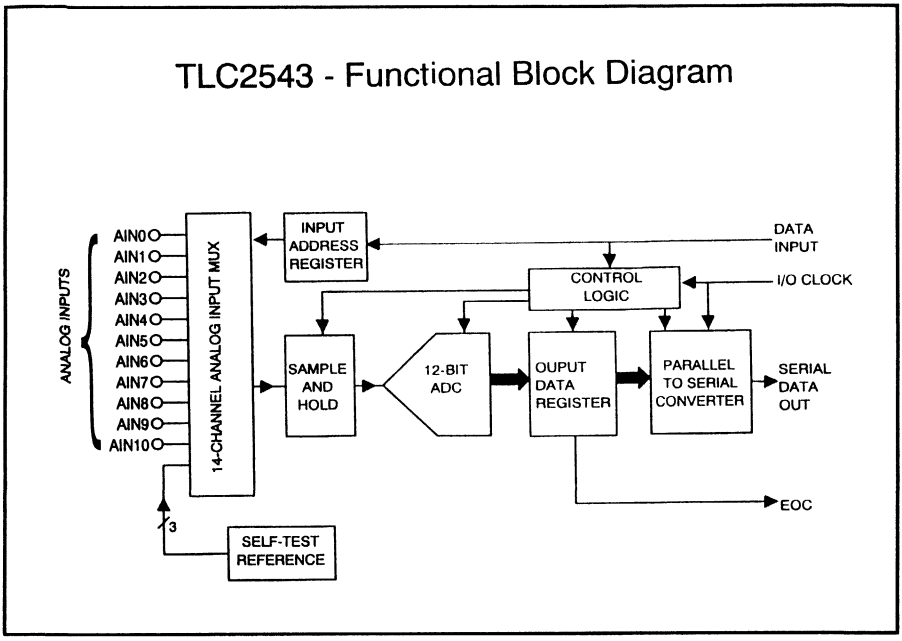

Figure 1.25 - TLC2543 - Functional Block Diagram

The internal architecture of the TLC2543 is shown in figure 1.25. The device includes a 14-channel input multiplexer, four channels of which are used by self-test modes. These modes allow the ADC to monitor the Vref+, Vref- and (Vref+ - Vref-)/2 values. These can be used as system checks. The input multiplexer is followed by an on-board sample/hold stage. The information held on the sample/hold is then passed to a switched capacitor successive approximation ADC core. On completion of the conversion an end of conversion (EOC) signal is output and the result is then transformed from parallel into serial data mode to be output at the DATA OUT pin. The ADC can be programmed to deliver the result in one of several data formats including MSB first and LSB first.

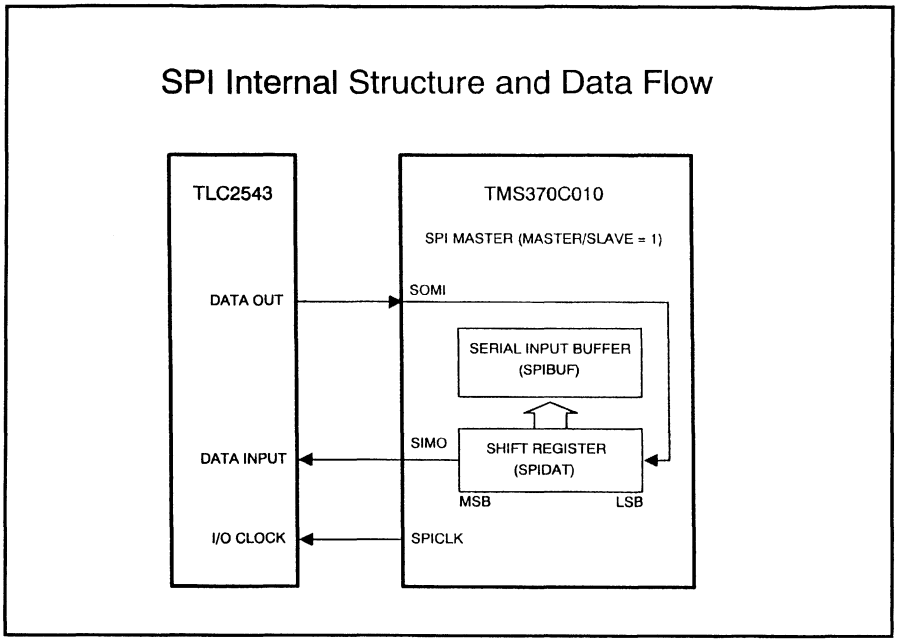

Figure 1.26 - SPI Internal Structure and Data Flow

When using the TLC2543 in sensor applications it is usual to control the mode of operation and the flow of conversion data using a microcontroller. Several methods of serial interface between microcontroller and TLC2543 are possible. However the most efficient is probably one which uses the SPI (Serial Peripheral Interface). Microcontrollers which include the SPI interface include the TMS370C10 and the MC68HC11.

The function of the SPI is illustrated in figure 1.26. It consists of an 8-bit serial shift register which is initially loaded by software with the mode-control data to be sent to the ADC input. The SPI transfer is then initiated by software. This automatically starts the output of serial data from the SIMO (Slave In Master Out) pin of the microcontroller. At the same time data from the previous conversion result is received at the SOMI (Slave Out Master In) pin of the microcontroller. This data is shifted into the other end of the serial shift register. On completion of an 8 bit SPI transfer the new contents of the shift register is automatically loaded into a serial input buffer ready to be read by the next software instruction in the routine.

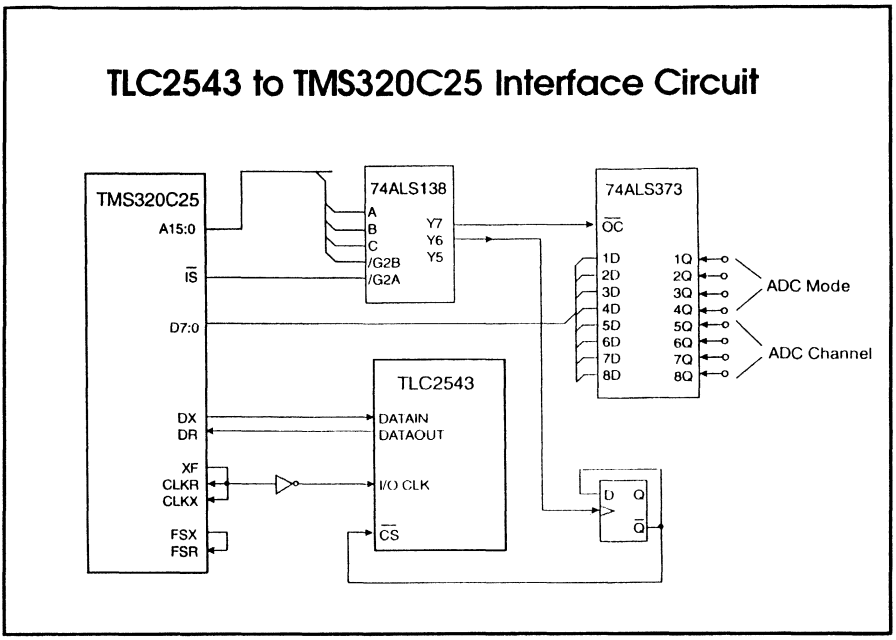

Figure 1.27 - TLC2543 to TMS320C25 Interface Circuit

Many 5-Volt sensor systems are now used in high speed closed loop control systems which rely upon the high computation speed of Digital Signal Processors to achieve their precision and stability.

It is important, therefore, to be able to transfer the conversion results from the ADC of the sensor electronics rapidly to the DSP. The interface shown in figure 1.27 can be used to achieve this transfer.

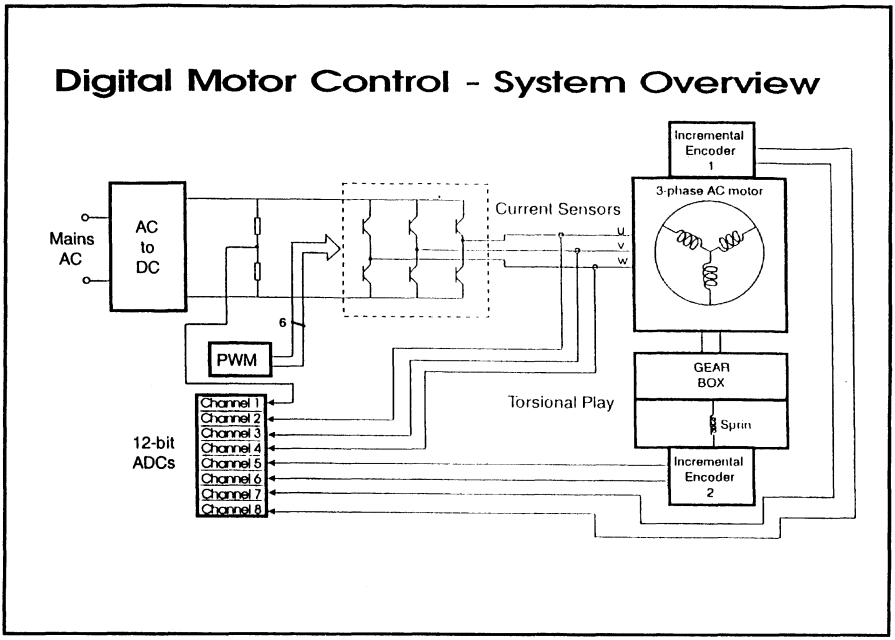

Figure 1.28 - Digital Motor Control - System Overview

An example of a closed loop control system which relies upon the rapid transfer of data from ADCs to the DSP is Digital Motor Control which is shown in figure 1.28. This method of motor control is used to accurately control the position of the rotor of asynchronous electric motors. This is achieved by sensing the instantaneous phase currents of the the stator windings using Hall sensors or similar techniques. These currents, in turn, indicate the instaneous magnetic fields which are present in the rotor windings. Knowledge of the direction and relative magnitude of these magnetic fields plus the instantaneous angular position of the rotor is sufficient to control the position of the rotor to the accuracy available from the position sensor.

The drive to each phase of the stator windings is provided by a pulse-width-modulated (PWM) synthesised sine wave. This PWM drive, which is provided by the DSP, closes the loop of the control system.

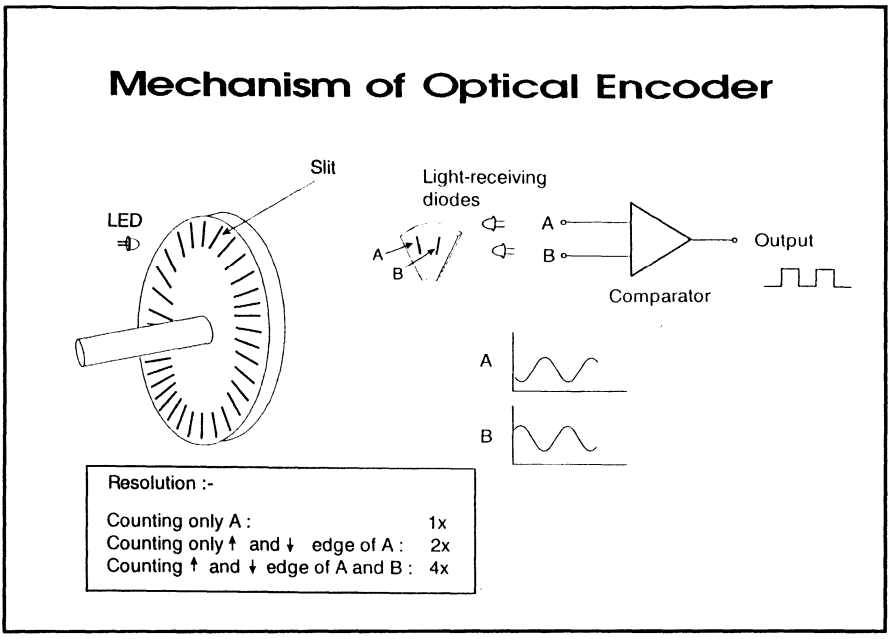

Figure 1.29 - Mechanism of Optical Encoder

A typical position sensor uses an optical encoder, the basic operation of which is shown in figure 1.29. The encoder consists of the wheel containing a number equally spaced slits positioned near its rim. The number of slits determines the coarse positional resolution of the system. Two light sensitive diodes or transistors are situated one side of the encoder wheel while a light emitting diode is positioned on the other side. The wheel is fixed to the shaft of the motor. As it rotates the quantity of light received by each diode is modulated as shown. The amplitudes of the light at A and B are converted into voltages and compared at a comparator. The output of this comparator yields higher positional resolution than the basic slit spacing as shon in figure 1.29.

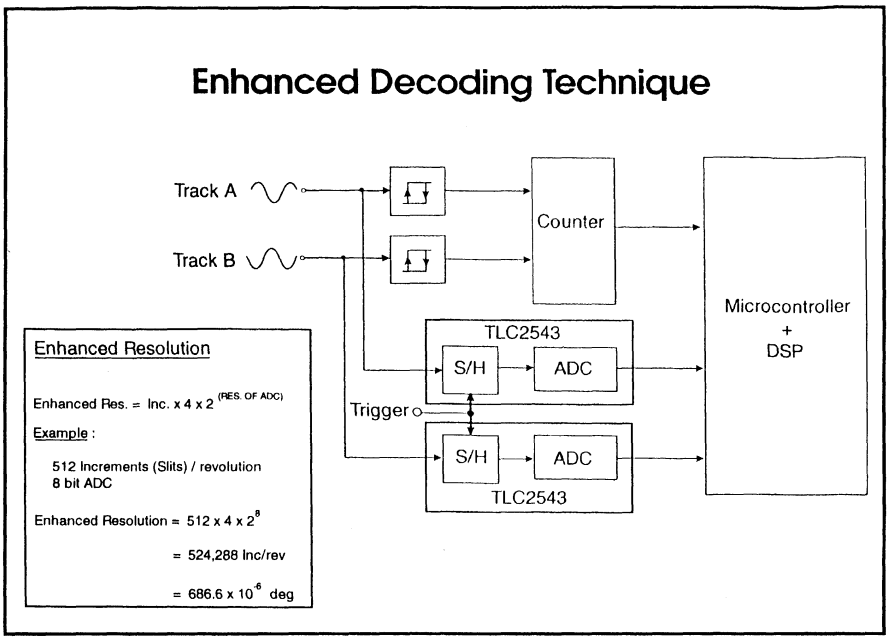

Figure 1.30 - Enhanced Decoding Technique

Enhanced decoding techniques exist which allow much high resolutions to be achieved from the optical encoder system previously described. Figure 1.30 shows such a decoding technique. This relies on measuring the instantaneous values of both track A and track B light receivers. The voltage levels of each track are converted into digital form and the results are fed into the DSP. Their relative magnitudes are used to compute the instantaneous position of the rotor to very high accuracies. For example a pair of 8-bit ADCs can be used to produce a positional resolution of 686.6 x 10^{-6} degrees. A pair of 12-bit ADCs will yield 16 times higher resolution.

These levels of performance may seem beyond the needs of normal requirements. However these very high angular resolutions become essential in applications such as robot arms where the radius of the rotation is long and the lateral translation produced by even minute fractions of a degree can be significant. This is particularly true in applications such as the assembly of automotive components where positioning to interference fit tolerances is commonplace.

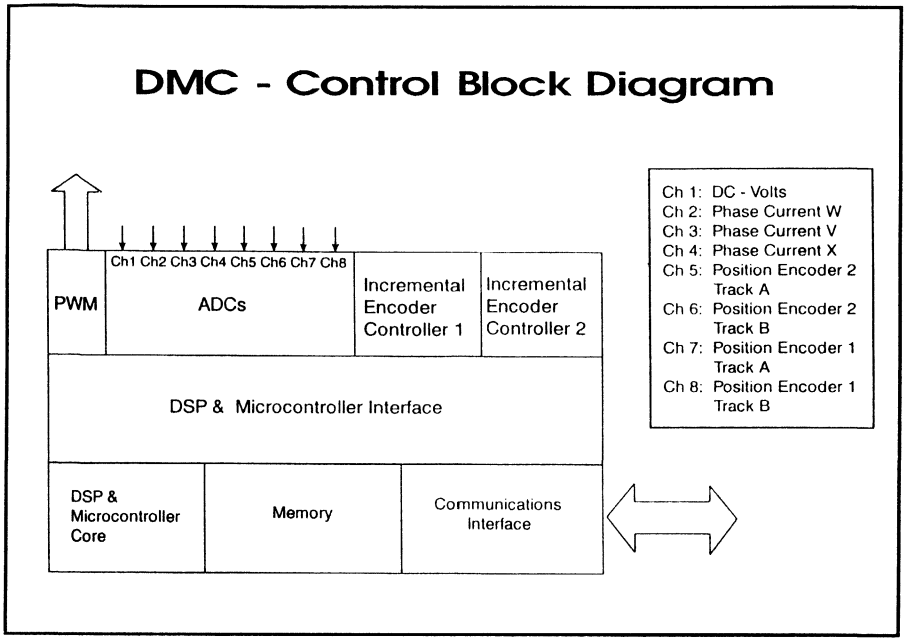

Figure 1.31 - DMC - Control Block Diagram

The overall control block diagram of a typical Digital Motor Control system is shown in figure 1-31. The two incremental optical encoders, one positioned at either end of the rotating plant , allow the control system to take account for torsional stres in the shaft and any play in the gearings and couplings which may be present in the system.

Eight ADCs are typically required to provide sufficient data to the DSP to control the rotor position. These include three ADCs to monitor phase currents, four ADCs to implement the enhanced position decoding and one to monitor the DC voltage from which the PWM sine waves are synthesised.

5 5-Volt Supply Data Converters

5.1 Introduction

The demand for analog-to-digital and digital-to-analog converters which can operate off a single 5-Volt supply is increasing rapidly. The following products meet some important application needs.

5.2 Video ADCs

Analog-to-digital converters which can convert at a rate in excess of twice the video bandwidth can be termed "video ADCs". One such device is the TLC5510 which converts at a minimum rate of up to 20 M samples per second. Its features, shown in figure 1-32 include an input bandwidth (-1dB) of 14 Mhz. This wide input bandwidth reduces signal distortion and ensures a linear conversion relationship between analog video signal and digital image processor.

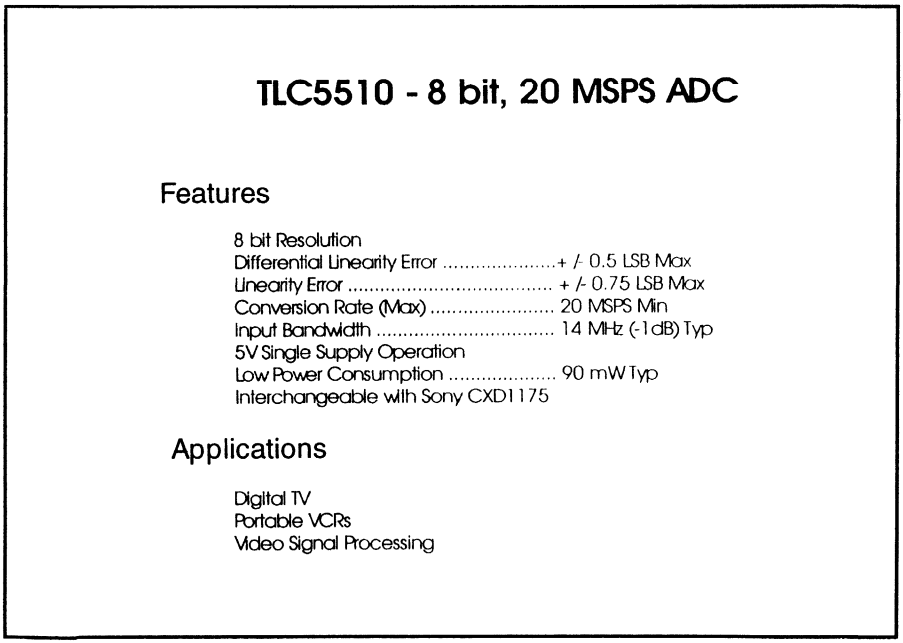

Figure 1.32 - TLC5510 - 8-bit, 20-MSPS ADC

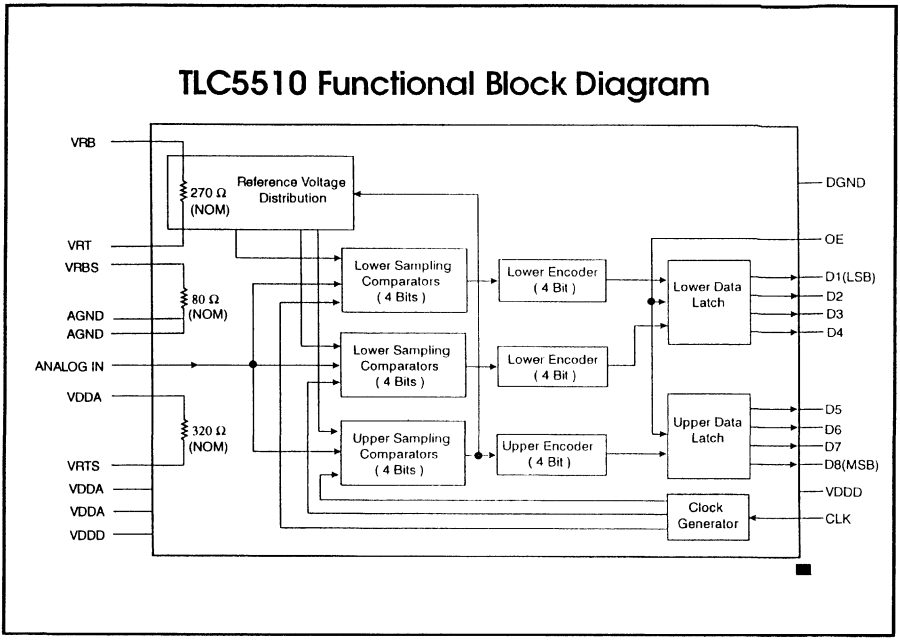

Figure 1.33 - TLC5510 Functional Block Diagram

The functional block diagram of the TLC5510 is shown in figure 1.33. It utilises a modified half-flash architecture which yields a faster results at lower power than that which would be achievable with the standard half-flash approach.

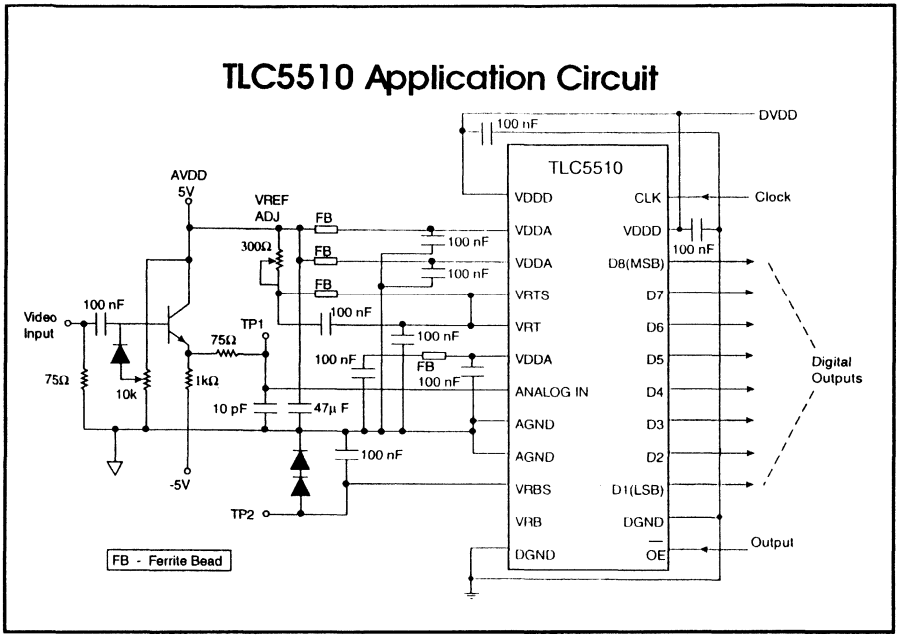

Figure 1.34 - TLC5510 Application Circuit

It is important when applying video ADCs to pay sufficient attention to grounding, decoupling and good layout of the printed circuit board. Figure 1.34 shows the typical components and their interconnect, **but not their layout**, which should accompany the TLC5510 in a video application. Frequent use of ferrite beads in the supply connections is recommended to increase the impedance to high frequency noise.

The transistor acts as an input buffer and provides level translation between the input signal and the +5-Volt single supply ADC.

5.3 8-bit DACs

The 8-bit digital-to-analog converter is now a ubiquitous electronic component which is used by system designers to perform many tasks which would have been out of the questions because of cost just a few years ago. Multiple DACs on a single IC save space and cost thus making their inclusion even more attractive to designers.

TLC5620 - Quad 8-bit Digital to Analog Converter

Features

Four 8-bit Voltage Output DACs
5-V Single Supply Operation
Serial Interface
Four Separate Reference Inputs
High Impedance Reference Inputs ..... 200 Kohms Typ
Programmable x1 or x2 Output Range
Simultaneous Update Facility
Internal Power-on Reset
Low Power Consumption ..... 10 mW Typ
Small Footprint - 14 pin SO package

Applications

Programmable Voltage Sources
Automatic Equipment Calibration
Automatic Test Equipment
Waveform Synthesis
Process Control

Figure 1.35 - TLC5620 - Quad 8-bit Digital to Analog Converter

The TLC5620 contains four voltage output 8-bit digital-to-analog converters on a single chip. Its main features which are summarised in figure 1.35 include a serial digital interface and simultaneous update facility. The gain of the output amplifiers which are connected to each DAC output can be programmed to either x1 or x2. There is an internal power-on facility which ensures that all DAC registers contain all zero's at device turn-on. Four separate reference inputs are available which provides maximum flexibility. All of this functionality requires only 10 mW of typical power consumption and is available in a space-saving 14-pin SO style package.

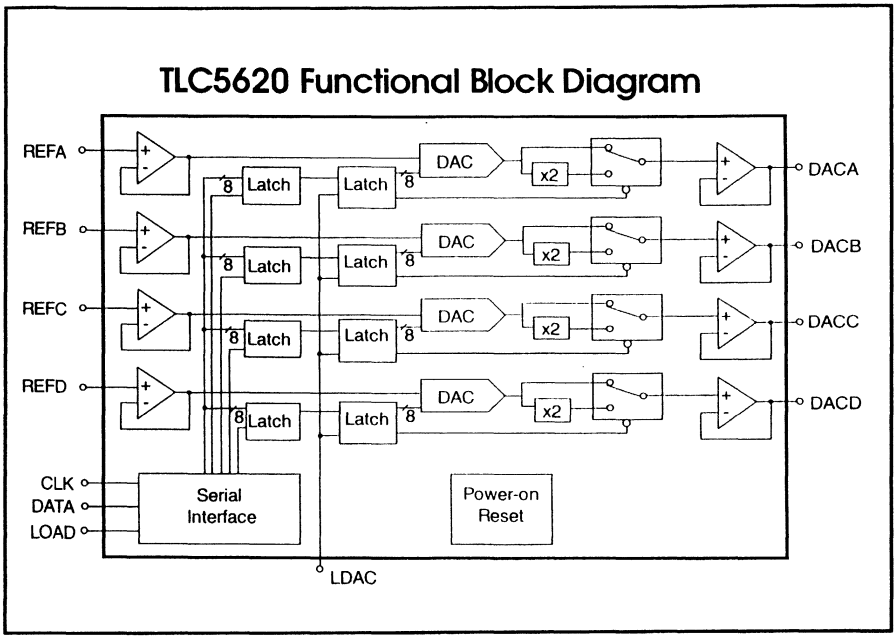

Figure 1.36 - TLC5620 Functional Block Diagram

The internal construction of the TLC5620 is shown in figure 1.36. The device is fully double-buffered which enables the first tier of latches to be loaded sequentially via the the serial DATA input and the second tier of latches to be loaded simultaneously by toggling the LDAC pin.

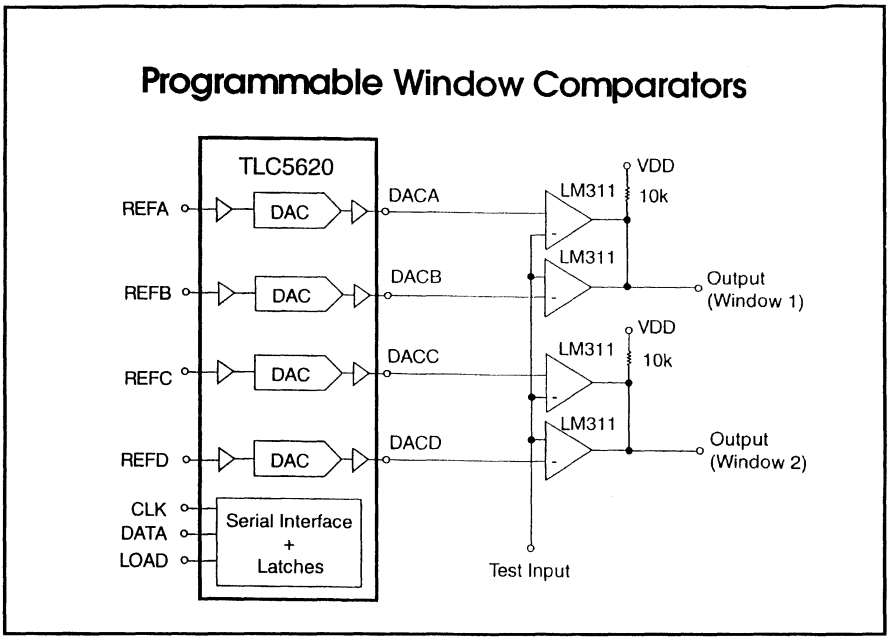

Figure 1.37 - Programmable Window Comparators

The applications of the TLC5620 include programmable voltage sources, automatic test equipment, automatic calibration routines, waveform synthesis and process control.

Figure 1.37 shows a pair of programmable window comparators which are used in automatic test equipment to determine pass/fail categories of components and/or systems. The open- collector outputs of the LM311 comparators are wire-ORed. Higher transition speeds may be achieved, if required, by reducing the value of the output pull-up resistors.

TLC5628 - Octal 8-bit Digital to Analog Converter

Features

Eight 8-bit Voltage Output DACs
5-V Single Supply Operation
Serial Interface
Two Reference Inputs
High Impedance Reference Inputs ..... 200 Kohms Typ
Programmable x1 or x2 Output Range
Simultaneous Update Facility
Internal Power-on Reset
Low Power Consumption ..... 20 mW Typ
Small Footprint - 16 pin SO package

Applications

Programmable Voltage Sources
Automatic Equipment Calibration
Automatic Test Equipment
Waveform Synthesis
Process Control

Figure 1.38 - TLC5628 - Octal 8-bit Digital to Analog Converter

The TLC5628 contains eight voltage output 8-bit DACs in a single 16-pin SO package. The features of the device are similar to those of the TLC5620 with only a few differences. These are highlighted in figure 1.38. The TLC5628 has twice the number of DACs as the TLC5620. The TLC5628 has only two reference inputs. It also consumes, quite understanably, twice the amount of power (20 mW typ) as the TLC5620.

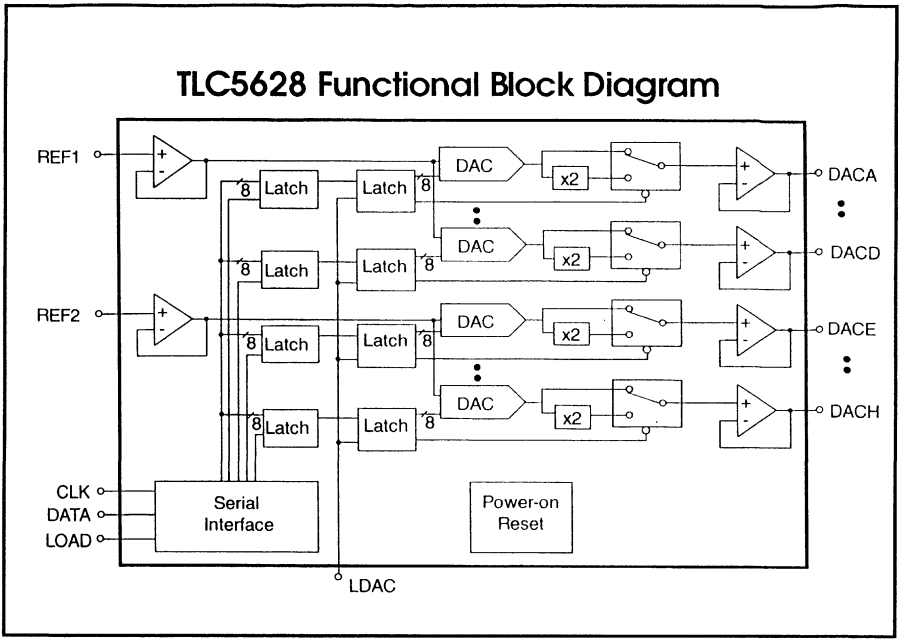

Figure 1.39 - TLC5628 Functional Block Diagram

The architecture of the TLC5628 is shown in figure 1.39. It shows a certain similarity to that of the TLC5620. The DACs are configured in two sets of four, each set being connected to a single reference input. However, like the TLC5620, all DACs can be loaded serially and updated simultaneously via a double-buffered data input structure.

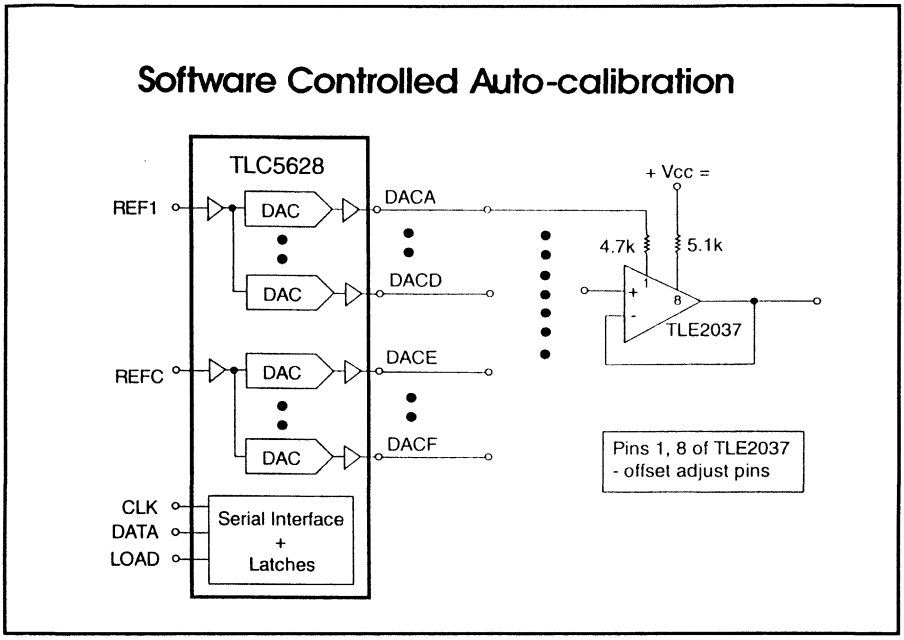

Figure 1.40 - Software Controlled Auto-calibration using the TLC5628 Octal DAC

The TLC5628 can be used in most of the applications previously mentioned for the TLC5620. Figure 1.40 shows how each DAC output can be used to adjust the offset of an operational amplifier in a software controlled auto-calibration system.

6 Grounding and Decoupling

6.1 Introduction

This next part of the seminar is important enough to warrant a separate section of its own. Unfortuneately we do not have time to cover all the many aspects of this subject. However it is worth mentioning some points which may help to improve system performance.

6.2 Grounding

The assumption by many design engineers that the word "ground" implies a zero-impedance return path where all good signals go to having completed their task in life is one which causes frequent problems in electronic systems. The situation is made worse in mixed-signal applications where high speed digital current spikes may share the same ground return path as sensitive analog signals.

The important point to remember is that every ground return path has a finite impedance associated with it. This means that it has a resistance, capacitance and inductance which can induce noise and instability in the system. This is often not a problem in purely digital systems. However in analog-only systems or, worse still, mixed analog-digital systems, poor grounding can ruin the performance of an otherwise good design.

To improve grounding the use of ground planes is recommended. This reduces the impedance of the ground return path significantly. It also makes this low impedance ground return path available to all the components on the printed circuit board. The use of matrix interconnect boards should be avoided in mixed-signal systems.

To enhance the performance of mixed-signal systems it is useful to separate the ground plane into two areas (at least). One area can be used exclusively as a ground return path for digital components such as logic, bus drivers and memory ICs. The other area is used as the ground return path for the more sensitive analog components. This has the effect of keeping potentially noisy high frequency digital currents from appearing in the ground return of the analog portion of the circuit. The two portions of the gound plane should only be connected prior to the return to the power supply.

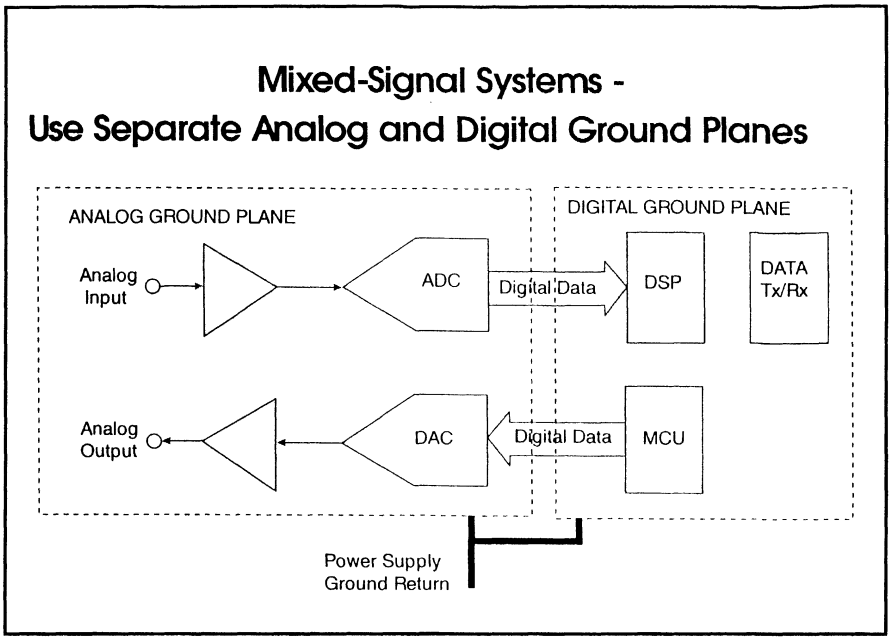

Figure 1.41 - Mixed-Signal Systems - Use of Separate Analog and Digital Ground Planes

Physical separation of digital ICs from analog components not only simplifies the provision of separate ground planes but also minimises capacitive coupling of high frequency digital signals to the sensitive analog portions of the printed circuit board.

6.3 Decoupling

The careful decoupling of both digital and analog ICs is essential to achieve optimum system performance in mixed-signal systems. The use of ground planes assists in providing a local route to ground, for every decoupling capacitor, anywhere on the PCB. It is suggested that a 100-nF ceramic capacitor is connected between the power supply pin of each device and the nearest point on the ground plane via short leads to reduce inductive effects. It is also worth connecting a tantalum capacitor of between 4.7 µF and 10 µF in value in parallel with the ceramic capacitor between the supply pins of particularly power hungry devices and the nearest point on the ground plane.

7 Intelligent opto sensors

7.1 Introduction

An important application for signal conditioning, is to amplify sensor signals from the outside 'real' world; and to generate appropriate signals for conversion to digital processing. In this section we consider techniques of measuring light and delivering these analogue measurements into the digital domain.

The simplest real-time measurement of light level is the simple photo-diode. In a photo-diode, incident radiation is absorbed by the silicon, to generate hole-electron pairs. These in turn give a photo-current across a reverse-biased p-n junction.

For a photo-diode current-mode sensor, the current is proportional to the light intensity.

Photo-diodes may be modified into photo-transistor elements or be used with appropriate op amps and then with data conversion elements to deliver a measurement of light level to a digital control circuit. In this section we shall examine structures which combine light sensing, signal conditioning and data conversion in integrated structures. Such devices will offer convenience of use at modest cost.

The Texas Instruments' LinCMOS™ process, used extensively for low input-offset operational amplifiers, can be easily adapted by the addition of light shields to make integrated photo-sensor structures. A photo-diode made by this process is responsive from 400 nm to 1100 nm (visible and short infra-red) when encapsulated in transparent plastic. The TSL250 and TSL230 integrated light sensors respond over this entire spectral range. However, by modified encapsulation a more restricted response (visible only, or infra-red only) can be achieved. An example of such a device is the TSL260.

7.2 Light-to-voltage sensors TSL250/TSL260

7.2.1 Overview

In this section, we shall describe how a current mode sensor is combined on a chip with relatively simple signal conditioning elements, to make a useful device. We shall consider the example of the TSL250 first. The TSL250 light-to-voltage converter solves some basic application needs. It is particularly suitable for analogue measurement of low light levels in an electrically noisy environment.

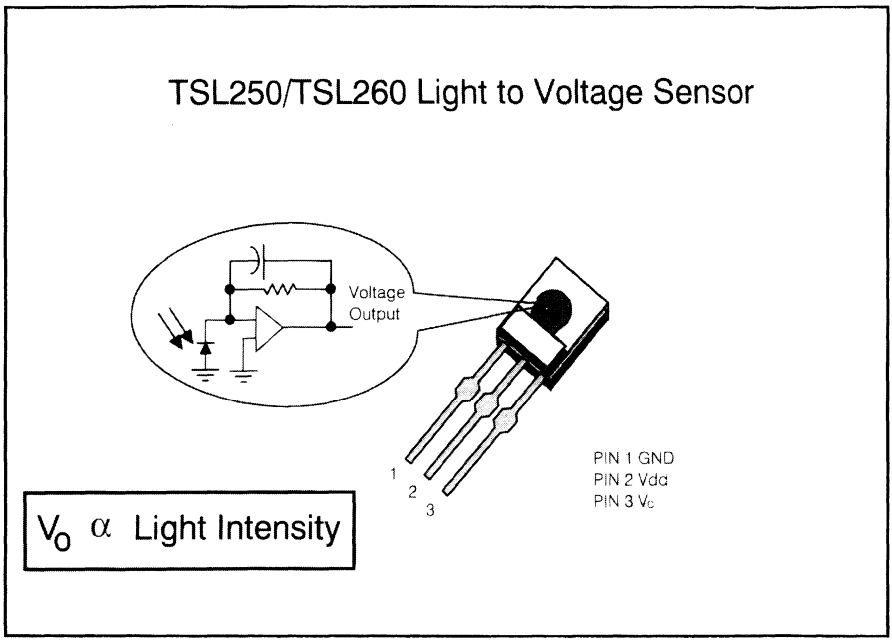

Figure 1.42 - TSL250/260 light-to-voltage sensors

In the TSL250, a large area photo-diode is combined with a trans-impedance amplifier, so the photo-diode current output is converted to an output voltage.

Three versions of the device are produced, with different photo-diode areas, and internal feedback resistor values.

7.2.2 Sensitivity Variants

TSL250 gives 2V output	for 25 microwatts/cm^2
TSL251 " "	for 60 microwatts/cm^2
TSL252 " "	for 425 microwatts/cm^2

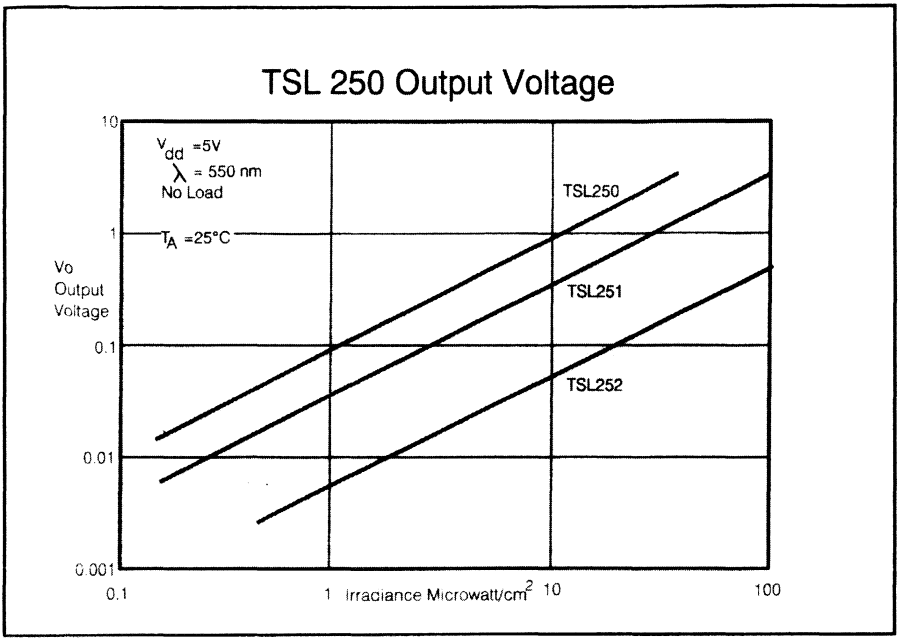

Figure 1.43 - TSL250 output voltage

To get some idea of what these incident light levels mean, we can consider a photo-metric equivalence (for visible radiation) of 90 lux = 14 μW/cm^2.

Dusk, when street lights are turned on, is about 70 lux. The TSL250 gives 2 V output at 150 lux. Office lighting at a work surface is typically 300-400 lux, where a TSL251 would give 2 V output. The TSL252 would give 2 V output in outdoor daylight illumination.

The TLS250 family is appropriate for a wide range of light sensing applications in light level control over a wide range of light levels, for security applications, and for boiler flame control in gas or oil heaters.

7.2.3 Characteristics

The LinCMOS™ trans-impedance amplifier (similar to the well-established Texas Instruments operational amplifier TLC272) provides stable low input offset. The TSL250 offers high dynamic range, with linear output up to 3V, with only 3 mV output in the dark.

The TSL250 has a significant advantage over discrete photo-diode light sensors under low illumination, since the high impedance output node of the diode is internal to the device. This makes the TSL250 inherently less sensitive to external electrical noise, so a highly stable sensitive detector can be realised without expensive and cumbersome screening techniques. Similarly the TSL250 is inherently less prone to current leakage problems in detector circuit assemblies.

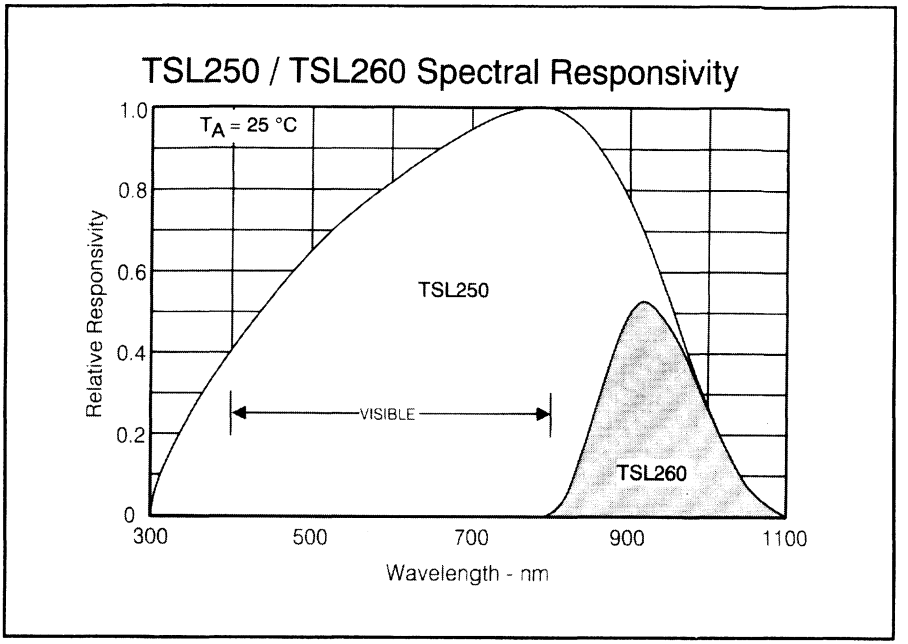

Figure 1.44 - TSL250/TSL260 spectral responsivity

In summary, the TSL250 family has a highly linear, stable, low-impedance voltage output. The TSL250 output is stable with temperature, changing by 1 micro volt per degree Celsius. This is because the temperature coefficient of the polycrystalline silicon feedback resistor compensates the temperature coefficient of the photo-diode.

The TSL250 operates off a single supply voltage (it is characterised at V_{DD} = 5 V , but will operate between 3 V and 9 V), and consumes little current (800 µA at V_{DD} = 5 V when illuminated).

The TSL250 family is offered in a high-volume clear plastic side looker package. For applications like infra-red remote control where the device should not be affected by ambient visible light, the same silicon die can be packaged in a light-blocking, infra-red transmissive plastic. The family of infra-red-only light to voltage sensors is the TSL260, TSL261 and TSL262. The sensitivity of these filtered devices is less, with the voltage output at the peak response wavelength approximately halved.

TSL250 / 260 Responsivity Variants

300 - 1100 nm	800 - 1100 nm
TSL250 - 25 μW/cm²	TSL260 - 48 μW/cm²
TSL251 - 45 μW/cm²	TSL261 - 87 μW/cm²
TSL252 - 285 μW/cm²	TSL262 - 525 μW/cm²

Input Irradiance for 2 V Output

Figure 1.45 - TSL250/TSL260 responsivity variants

7.2.4 Speed Vs Responsivity

The internal feedback in the trans-impedance amplifier increases from the TSL252 to the TSL250. As the feedback is increased the speed is reduced. The TSL252 output rise and fall times are typically 7 μs, for the TSL251 they increase to 90 μs, and for the TSL250 they are 360 μs. In the TSL260 family the response time of each device corresponds to its unfiltered (TSL250) equivalent. For example the TSL261 has the same output rise and fall times as the TSL251.

The basic die design could be extended to higher speed operation, trading responsivity for speed, by reducing the diode area and the feedback resistor and capacitor values -- the extremely low dark voltage resulting from the LinCMOS™ technology would permit this.

7.2.5 TSL250/TSL260 Data conversion

From a 5-V supply rail the TSL250/TSL260 families give a linear output up to approximately 3 V, and saturate typically at 3.5 V. Use of a pull-up resistor can extend the linear output range to within typically 10 mV of the positive supply rail, with a penalty of only a few milli-volts increase in the dark level output. A TSL250 or TSL260 can be combined with an appropriate ADC to deliver light measurement to a digital processor.

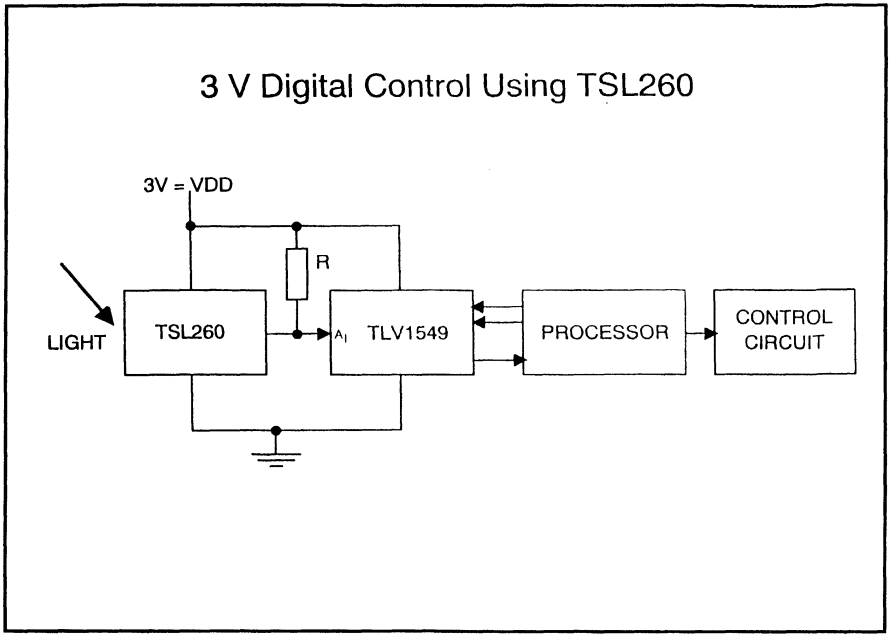

Figure 1.46 - Digital control using the TSL260

A simple schematic is shown, see figure 1.46, combining the TSL260 with the 10-bit serial input ADC TLV1549. A pull-up resistor is used to give a good dynamic range from a nominal 3.3-V positive supply rail. The lowest dark level is obtained by use of a high pull-up resistor value, but this exacts a penalty in conversion speed. A resistor value of 100 kΩ will allow measurements of low light level, since the dark current level is typically 3 mV; however the conversion speed will be only 300 Hz. To run the TSL262 at its maximum speed with this simple circuit the resistor value would need to be reduced to 1 kΩ and the dark current level would increase typically to 15 mV.

The next device we shall consider operates through a different principle and is capable, at modest cost, of giving high resolution, linearity and speed.

7.3 Light-to-frequency sensors TSL230

7.3.1 Overview

Next we shall examine a high performance and low cost technique of delivering the output from a light sensor into the digital domain. Instead of classic conversion of an analogue sensor output through an A-D converter (either discrete as in the example of the TSL260 and the TLV1549; or with the A-D converter integrated into a micro controller, or sensor system processor like the TSS400) a photo diode current can be converted into a frequency output. This output can be handled by a counter or timer.

Thus high precision light measurement can be accomplished without the cost of separate analog to digital conversion.

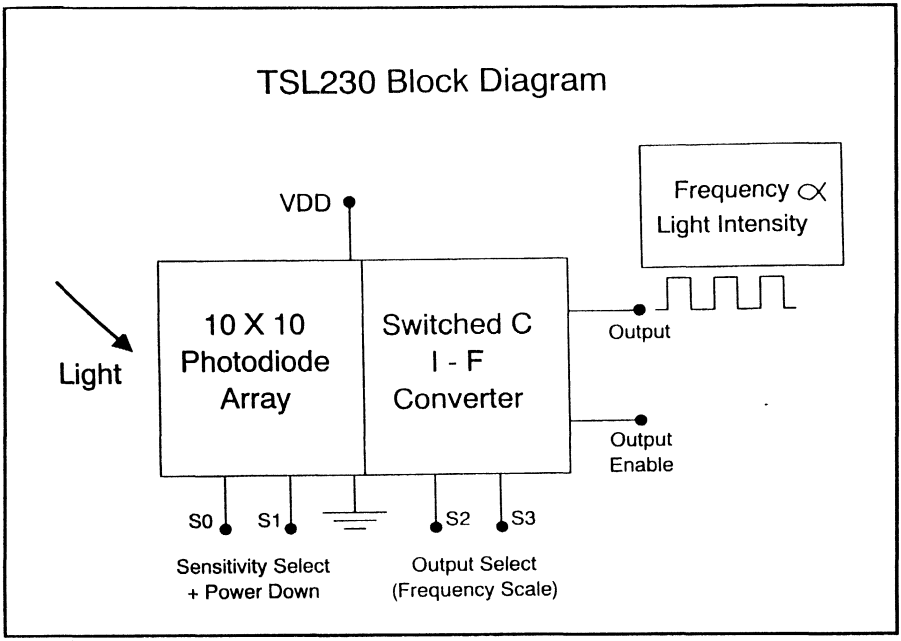

Figure 1.47 - TSL230 block diagram

The device to realise this is a low-cost programmable device, the TSL230. This enables a wide dynamic range of light level to be measured with high precision, linearity and temperature stability; or rapidly changing light levels to be processed. The TSL230 can be directly coupled to a digital processor, in micro controller, or logic control as the application dictates.

7.3.2 TSL230 Characteristics

The TSL230 is a monolithic programmable light-to-frequency converter. It is currently the only device of its kind to offer direct high resolution conversion of visible and short infra red radiation into digital format.

It contains an array of 100 photo diodes with a patented current-to-frequency converter (using switched capacitor charge metering). The output is a pulse train, with frequency proportional to the light intensity incident on the active photo diode area. Input lines from the digital control circuit provide real-time control of the TSL230 sensitivity (unlike the earlier TSL220 device no external capacitors need be provided) and offer a power-down function; also the output frequency can be scaled to match the characteristics of the digital control circuit. For stable or slowly changing light levels, very high resolution may be obtained by pulse counting; for rapidly changing light levels the pulse separation may be timed.

The TSL230 operates from a single supply (from 3 V to 6 V) drawing typically 2 mA supply current. These is a pin-programmable power-down option, reducing the supply to 10 micro amps when the sensor is not active. This is useful for portable, battery powered applications.

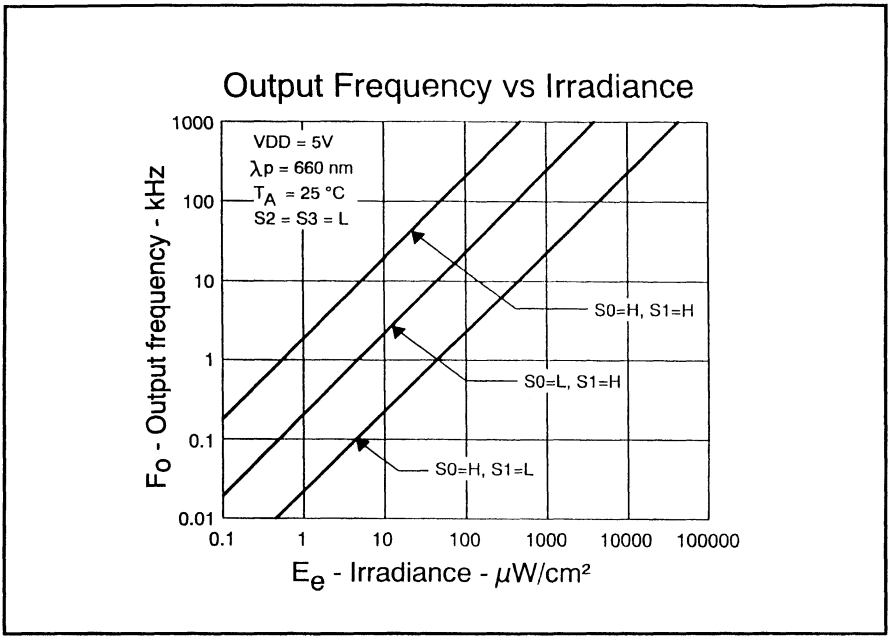

Figure 1.48 - TSL230 output frequency vs irradiance

The programmable sensitivity of the TSL230 is effected by a simple electronic technique, switching in different numbers of the 100 elements of the photo diode matrix. These sensitivity ranges (X1, X10, X100) can be chosen through the logic levels of input pins S_0 and S_1. The digital control circuit can thus optimise the TSL220 operation to the ambient light level, preserving the full output frequency range. The light levels of 0.001 to 100,000 μW/am² can be accommodated directly, without the expense of filters.

For cost reasons, low cost micro controllers with limited frequency range may wish to be used for the digital control circuit. The TSL230 has two input lines S_2 and S_3 to provide output frequency scaling. Options are an undivided pulse train with fixed pulse width, or square wave divide-by-2, -10, or -100 outputs. There is also an output enable pin, so that the TSL230 can be placed in a high impedance state when not required. This is useful for applications where several input devices share a micro controller.

The TSL230 is temperature compensated to give a stable 300 ppm change in output frequency per degree Celsius (at 660 μm radiation).

The non-linearity error is low; being typically only 0.2% full-scale for the output frequency range 0 to 100 kHz. Dark output is typically only 1 Hz.

The TSL230 is offered in a transparent 8-pin Dual-In-Line package. It is highly versatile and suitable for a wide range of light-measuring and position-detecting applications.

The pulse output gives the TSL230 high noise immunity, making it suitable for industrial environments.

Typical applications of the TSL230 include water turbidity measurement, flame control in heaters, light-metering, fluid absorption measurement, paper handling, and general visual process control.

For slowly changing or stable light sources, the wide dynamic range of the TSL230 enables high precision measurements to be made. Further, since the TSL230 output responds pulse by pulse, the device can also sense quickly changing light sources. An application brief (SLBT003 - TI Library Ref) demonstrates how to take 16-bit or 8-bit measurements using 3 popular microcontrollers from Texas Instruments, Motorola and (Arizona) Microchip. Program listings are given.

7.3.3 TSL235 Pre-programmed Light to Frequency Converter

It is clear that for the essential light to frequency conversion function only three connections are required - the voltage source, the ground and the output. To reduce user cost even further a pre-programmed variant -TSL235- is offered in a low cost, three terminal sidelooker package. This package is identical to that used in the TSL250 light to voltage converter described earlier. In the TSL235 the photodiode array is preprogrammed so that all one hundred elements are always used. The output frequency divider is also fixed in the divide-by-2 setting which gives a square wave output. The TSL235 thus operates up to 500 kHz maximum output frequency and preserves most of the dynamic range of the TSL230.

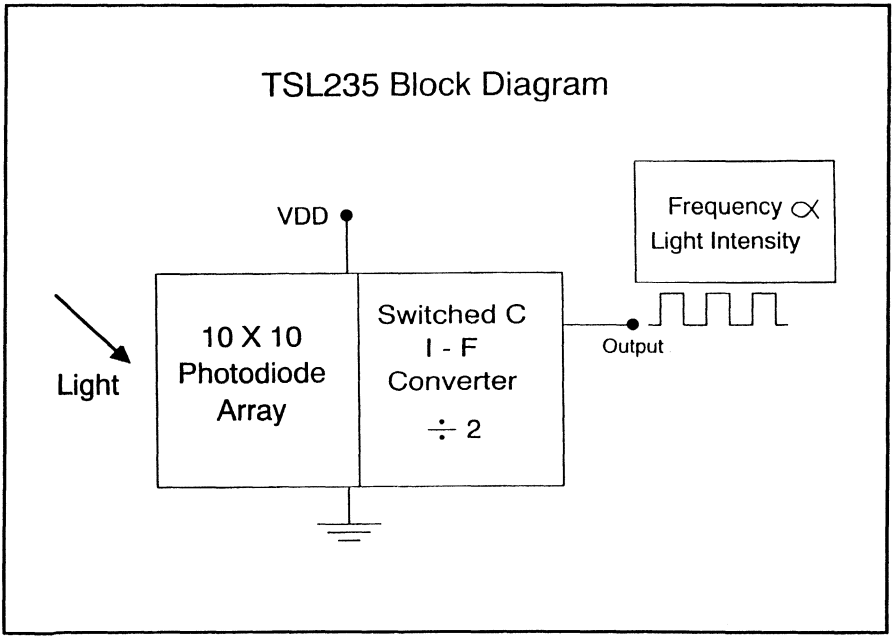

Figure 1.49 - TSL235 Block Diagram

7.4 Line arrays - TSL213/TSL215

7.4.1 TSL213 Functional Block Diagram

7.4.2 Summary

The TSL213 array illustrates how a complex sensor, which integrates light-sensing , analogue and digital elements, can offer the prospects of low system cost, and ease of design.

The TSL213 is a 64-element line sensor, fabricated from the established Texas Instruments LinCMOS™ mixed-mode volume wafer technology. The pixels have a 125 micron centre-to-centre spacing. The TSL213 is a charge-mode sensor. That is, during an exposure period, a charge is developed on each pixel proportional to the product of the light intensity and the exposure time (in this it is like a CCD imager, and analogous to photographic film).

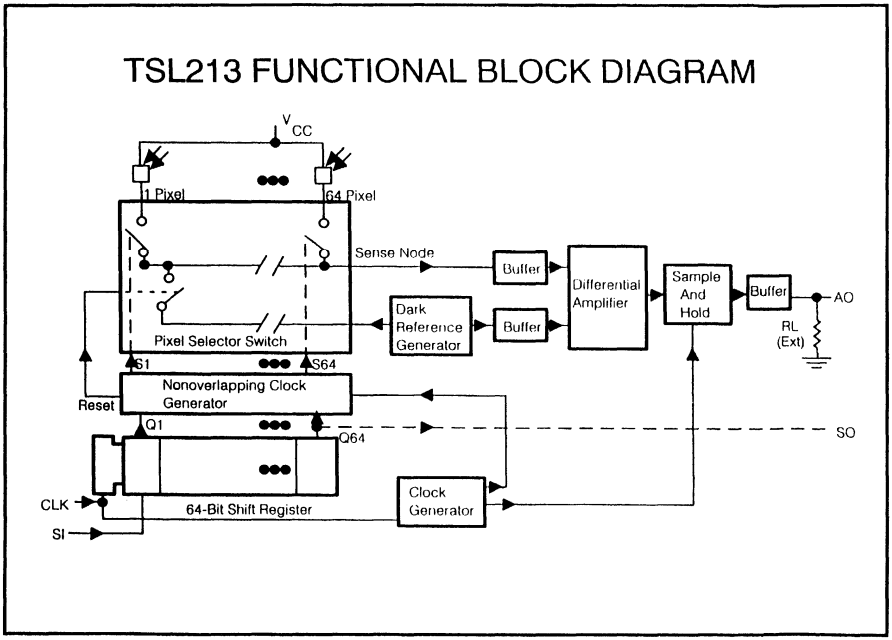

Figure 1.50 - TSL213 Functional Block Diagram

On a single TSL213 die are integrated the light-sensing pixels, analogue signal conditioning, and digital address and switch elements (equivalent to approximately 2500 gates).

The internal complexity of the die has been chosen, to make the device easy to use in a microprocessor or digital processing system environment. To operate the TSL213, only a single 5V supply and integration (exposure) and pixel output clock pulses are required.

7.4.3 Characteristics

The TSL213 operates at data rates between 10 kHz and 500 kHz. The relatively large pixel size permits assembly in a high volume low cost 14-pin plastic dual-in-line package.

The TSL213 is recommended as a real alternative to either discrete photo-sensor arrays or to CCD line imagers in sensing systems where more than one sensor is required, and the sensors form part of a digital control system. Typically the pixel size in a line CCD imager is 10 microns, and for a discrete photo-diode or photo-transistor is 1000 microns. At 125 microns pixel size, the TSL213 is appropriate for many applications.

7.4.4 Function Blocks

The functional structure of the TSL213 is shown in Figure 1.50. There are 64 pixels in a line array, which are addressed individually (unlike CCD where all pixel charges are switched along an analogue register simultaneously).

The exposure or integration period is defined as the time between clock pulses on the Serial Input (SI) pin. The integration period is chosen in each application to give a suitable output level for the light intensity available.

The charge in each pixel is transferred to the output sense node by means of the Clock Pulse (CLK). The sense node generates a signal voltage directly proportional to the charge.

A 64-bit shift register controls the transfer of charges to the output and provides timing signals for the non-overlapping clock generator (NOCG). The NOCG provides internal control for the sensor elements, including charge sensing and reset. The reset establishes a known voltage at the sense node in preparation for the next pixel charge transfer. This voltage is used as a dark reference level for the differential signal amplifier. By means of the NOCG, feedthrough clock noise is eliminated at the output. The sample-and-hold signal generated by the NOCG holds the voltage analogue output of each pixel constant until the next pixel is clocked out.

7.4.5 TSL213 Timing Diagram

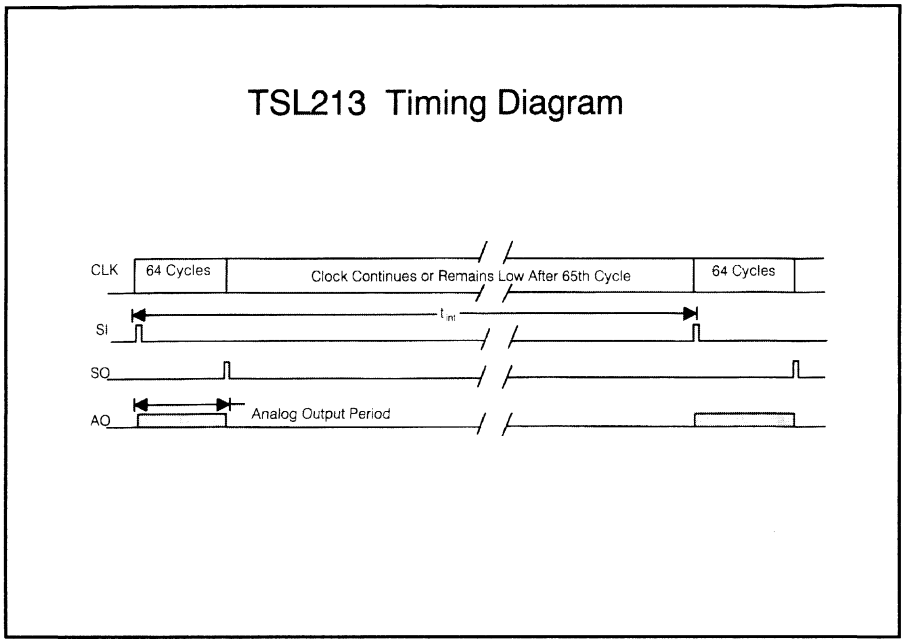

Figure 1.51 - TSL213 Timing Diagram

7.4.6 Combination Of Arrays

The architecture of the TSL213 enables more than one array or die to be connected in series or parallel configuration. Thus a 128 pixel device (TSL215) may be easily created. The 64 pixels of the TSL213 die are in groups of 8 pixels; the outputs of different groups may be balanced by means of resistors which can be fused to one of 5 levels at multi-probe. This enables long uniform arrays of pixels to be realised -- practical 1728 pixel 200 dpi A4 facsimile contact sensors can be made by serial connection of TSL213 dice.

Several TSL213 imager die may be connected in series or in parallel, on customised substrates to provide higher complexity imagers. For example, eight serially connected dice could make a 512 pixel line imager, for a mark reader such as a lottery card reader.

Serial Connection

For serial connection, the Analogue Outputs (AO) must be connected together and the Serial Output (SO) of each sensor array connected to the Serial Input (SI) of the next array. The externally applied SI pulse is applied only to the first array of the series. For n arrays in cascade the SI pulse is applied after each n x 64 positive going clock transitions.

Parallel operation

Parallel operation of multiple arrays is achieved by supplying clock and SI pulses simultaneously. The outputs of each device may then be processed separately.

Initialisation

At power up, or after a period of SI or readout clock inactivity exceeding the integration time, the sensor elements may need to be initialised. This consists of 15 consecutively performed output cycles to clear the pixels of any charge which has accumulated during the inactive period.

7.4.7 TSL215/TC102 Comparison

Summary

Two TSL213 dice may be combined serially within a single device to make the TSL215 128-pixel line sensor array. The TSL215 is here compared with a 128-pixel CCD line array , the TC102.

Pixel Size

The most obvious difference is that the active optical length of the TSL215 is almost 10 times that of the TC102. The TC102 is a CCD array where all the pixel charges of an integration period are clocked out together down transport registers, while the TSL215 is an addressed array where pixel charges are individually switched out. The coarser pitch of the TSL215 derives from the physical size of the switching elements (including the NOCG) associated with each individual pixel. For the standard LinCMOS™ technology the relatively fine optical resolution of the CCD cannot be realised.

Comparison of 128 Pixel Imagers

	TSL215 (Addressed Array)	TC102 (CCD Imager)
Pitch Speed	125 micron 1MHz o/p data	12.7 micron 10MHz o/p data
Input	5V digital supply, integration & readout clocks	+2V, -16V clock +16V VDD, +7V REF. Needs mos-drivers (Ext.)
Readout	Pixels individually addressed	All pixel charges simultaneously moved
Output Conditioning	Analog video output	Needs video clamp, external sample/hold to remove clock noise.

Figure 1.52 - Comparison of 128-pixel Imagers

Data Rate

The maximum data output rate of the TSL215 has been set by the switching design at 1MHz, whereas with careful driver circuit design the TC102 can deliver data out at up to

10 MHz. However, the TSL215 is far simpler and more economical to drive, and its output is more easily handled.

Drive Requirement

The TSL215 drive requirement is a single 5 V supply, an integration pulse and a output clock . The TC102, however, requires positive (+2 V) and negative (-16 V) clock pulses, +16 V V_{DD}, and a 7-V reference. The registers must be driven through a dual MOS-driver such as the TLD369.

Output Requirement

The output of the TSL215 is also much more convenient , being an analogue video envelope. With the TC102, the analogue voltage levels of the video pixels are offset by the output buffer amplifier, and must be externally clamped to a video black reference using a train of black reference pixels provided. External sample-and-hold must be done on the clamped voltage output, to eliminate the clock feedthrough noise between the valid pixel levels.

Cost

These input and output tasks with the CCD device make it much more expensive in a system, on top of the higher cost of the CCD device itself. (One advantage of the relatively coarse pixels is that a low cost plastic packaging technique may be used). For applications where arrays of discrete photo-sensors, or low resolution CCD were hitherto used, the TSL213/TSL215 provides an attractive alternative.

7.4.8 PC404/PC405 - Evaluation Systems

Evaluation kits, PC404/PC405, are available to facilitate initial evaluation of the TSL213 and TSL215 Line Arrays. They also demonstrate the simplicity of operation of the arrays with digital control circuits to perform complete light sensing functions.

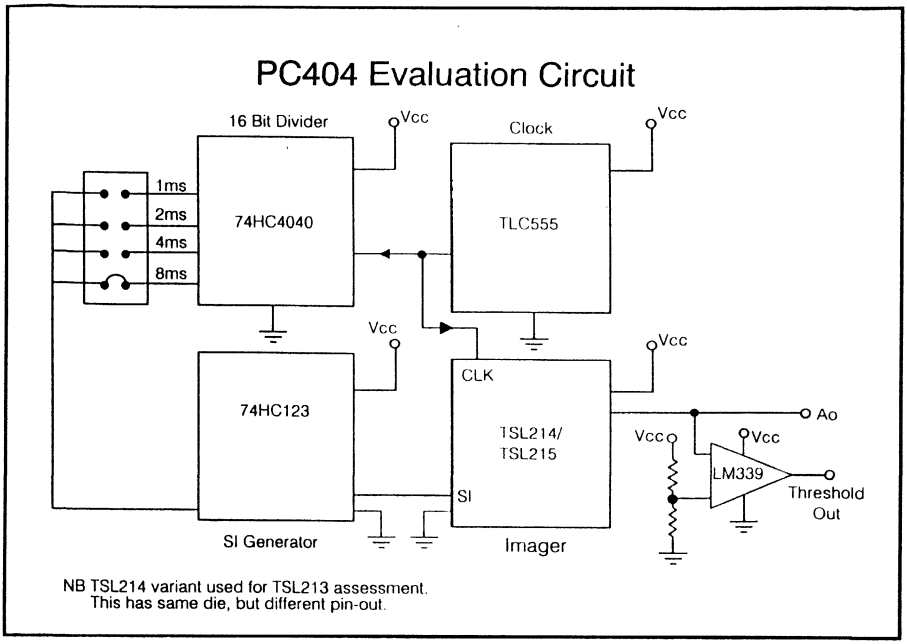

Figure 1.53 - PC404 Evaluation Circuit

PC404 Kit

The PC404 consists of an imager, a circuit board with drive and output circuitry, and a detachable 10 x magnification lens in a housing. The circuitry of the PC404 comprises an oscillator, a counter/divider, a one-shot pulse generator and a comparator. The oscillator is built round a TLC555 timer and generates a 500 kHz output data clock pulse. the clock output of the oscillator is routed also to a 74HC4040 divider. This has a set of jumper terminals to four of the outputs, and 1 ms, 2 ms, 4 ms or 8 ms Integration Time may be selected. The chosen output is connected to the 75HC123 one-shot pulse generator, which provides the imager with the SI pulse.

Trimming potentiometers and test points are provided. Two alternative outputs are provided. One is the Analogue Output (AO); for the other - Threshold Out - the AO is routed to an LM339 comparator, which squares up the output for digital compatibility.

PC405 kit

The PC405 board is software based. A pre-programmed 8 bit micro controller provides the drive to the line imager, processes the imager output and drives a two-digit LED output display.

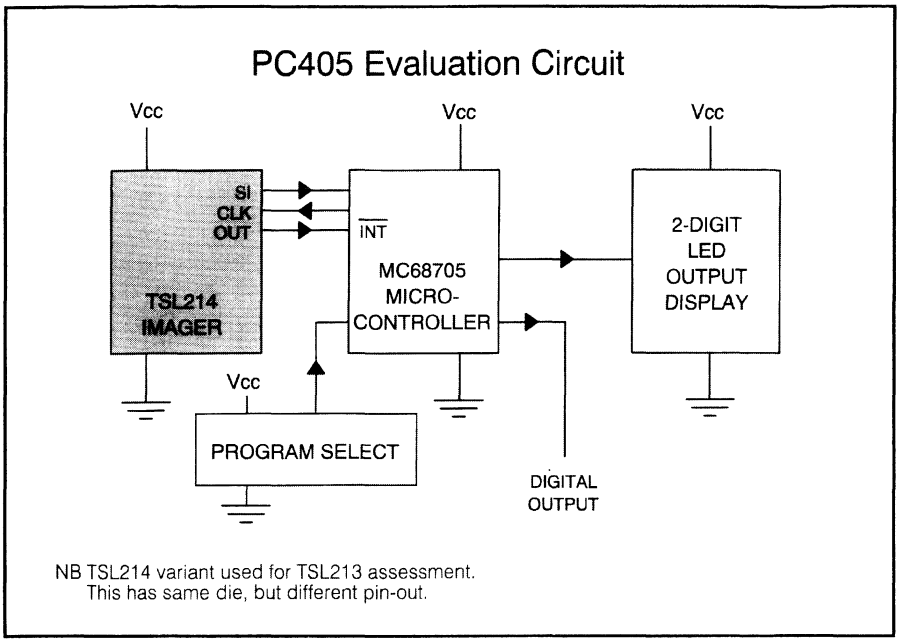

Figure 1.54 - PC405 Evaluation Circuit

Four functions are available:

- Digital Output
- Object Edge Detection
- Line Position Detection
- Light/Dark Transition Counter

Section 2
Analog Interface Circuits

Section Contributions by:
John Walliker of UCL
Julian Daley of UCL
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Edited by: Elwyn Davies

TEXAS INSTRUMENTS

Contents Section 2

1 Introduction

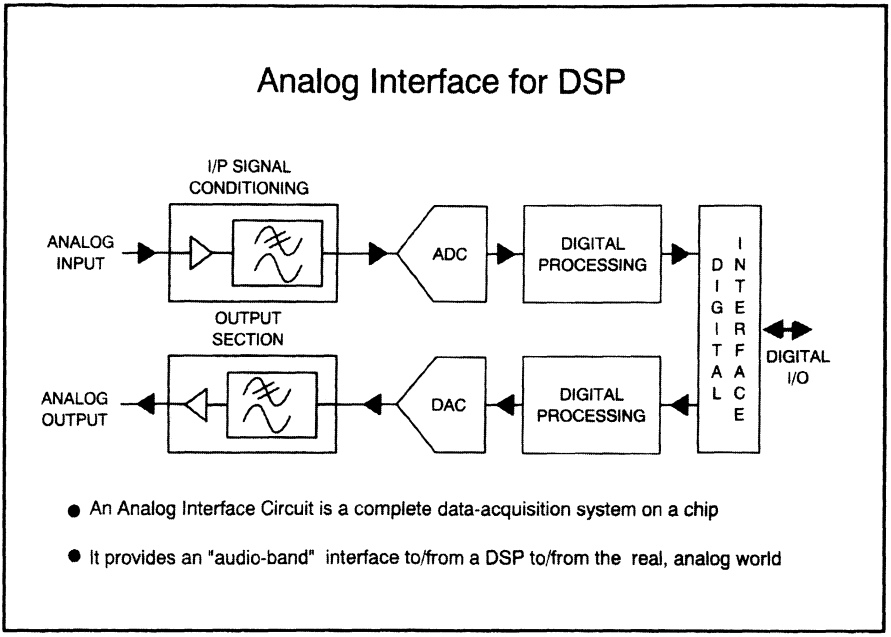


Figure 2.1 - Analogue Interface Circuit in a DSP Based System

The last decade has seen the adoption of digital signal processing (DSP) techniques in a whole range of industrial and consumer products. The advantages of accuracy and repeatability of digital approaches are being utilised in functions ranging from multi-tap filters in communications systems through to precision motor control.

A fundamental requirement which remains necessary, in order to expoit DSP methods, is the conversion of signals from analogue into digital and digital into analogue form and the rapid transfer of these conversion results into and out of the digital signal processor. It is important that bottlenecks are avoided in the flow of data between the real world and the computational heart of the DSP. The Analog Interface Circuit is a class of mixed-signal products which includes the necessary analog circuit blocks and an optimised interconnection scheme to facilitate the rapid and efficient transfer of information between the analog and digital domains.

2 Voice Band Audio Processors

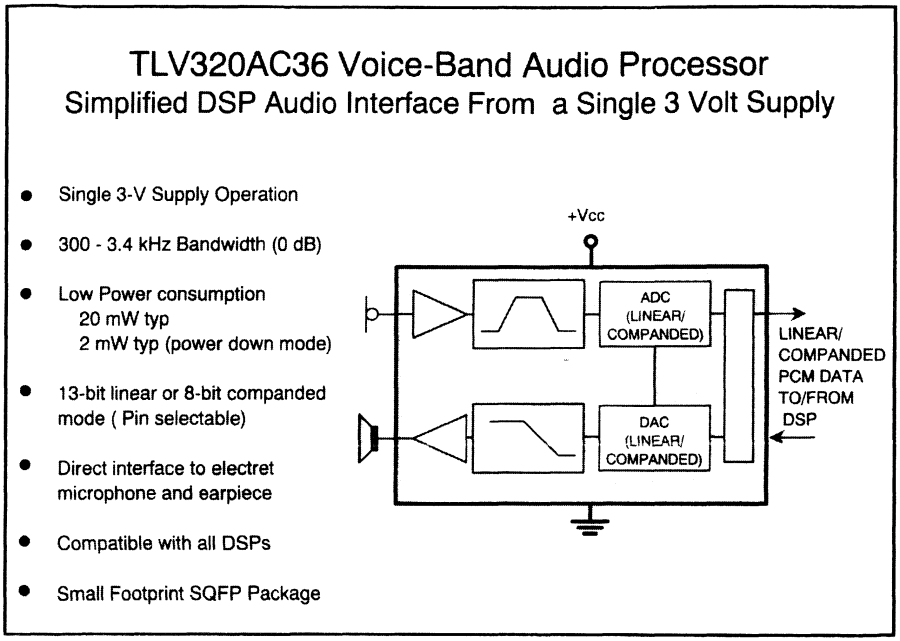


Figure 2.2 - The Voice-band Audio Processor

2.1 Introduction

Many voice-band signal applications now require an efficient interface between analog components and the DSP in order to save space, weight and power consumption in an increasingly portable world.

This need has spawned a significant family of AICs known as Voice-band Audio Processors or VBAPs. Like other more conventional AICs, they offer ADC, DAC, pre and post filter stages and on-chip amplifiers, as shown in figure 2.2. However, the electrical characteristics of these sub-components have been tailored to meet the specific needs of voice-band applications. Texas Instruments has developed the TCM320AC3X/4X family of monolithic ICs which provide the complete voice-band (200 Hz - 3.6 kHz) interface and operate with a 5-V single supply. Recently the range of VBAPs has been expanded to include the TLV320AC36 which requires only a 3-V single supply voltage.

The devices are suitable for a wide range of voice-band data acquisition systems using a DSP including cellular and cordless telephones, answer machines and test equipment.

2.2 The TLV320AC36 3-V Supply VBAP

At present 5 volts is the supply voltage of choice for mobile phones and other VBAP™ applications though manufacturers are looking seriously at moving to 3 volts for new designs to reduce power consumption and increase battery life. The TLV320AC36 3-V VBAP is already available to meet that need. The device utilises both continuous time anti-aliasing and switched capacitor low pass filters to pre-condition the input signal prior to analog to digital conversion as shown in figure 2.3.

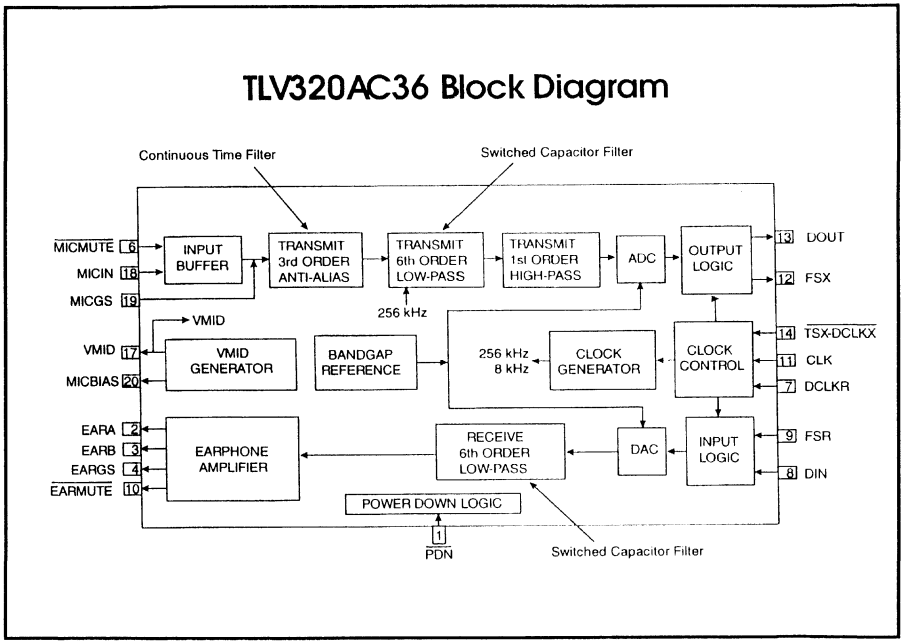


Figure 2.3 - TLV320AC36 Block Diagram

The TLV320AC36 offers user-programmable linear and μ–Law companding data conversion and runs with a master clock of 2.048 Mhz. The device consumes only 20 mW in normal operating mode. This is reduced to only 2 mW when the power down facility is activated by taking the /PDN pin low. Its suitability to mobile phone applications has been further enhanced by the recent introduction of the plastic quad flatpack version (PT) which has a footprint of less than 1 cm square (including leads) and a height above the PCB of less than 2 mm.

The TLV320AC36 is similar in architecture to the other members of the VBAP family. It is useful to review their common features.

2.3 Voice-band Audio Processor Building Blocks

The Voice-Band Audio Processor (VBAP) is divided into a transmit and receive section which is controlled from a central timing unit. The input signals from the microphone are amplified via a programmable gain input amplifier to accommodate a range of signal input levels. The amplified signal is passed through an anti-aliasing filter and a high pass filter then converted into digital code. The linear selection pin, when LOW, selects 13-bit linear coding/decoding and, when HIGH, selects companded coding/decoding. Selection of the linear mode of operation reduces the software required in the DSP. The digital data is buffered and clocked out, to the DSP, via the output logic.

The received digital signals are clocked into the device via input logic. The status of the linear selection pin, /LINSEL, determines if the incoming data is companded and requires decoding or if the data may be transferred directly to the DAC. The analog signal from the DAC is passed through switched capacitor filters, which provide out-of-band rejection and (sinx)/x correction. Switched capacitor design techniques provide the user with precise audio band pass filtering and low power consumption. The filtered signal is presented to the differential output amplifier which may be connected directly to a piezo speaker.

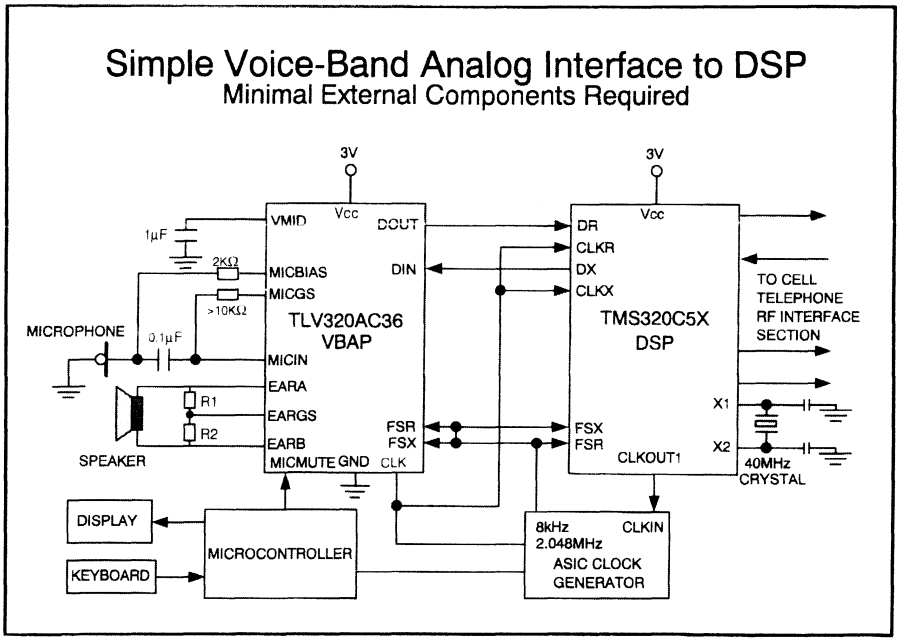


Figure 2.4 - Simple Voice-band Analog Interface to DSP

Both the input and output amplifiers have a mute function which is accessible by the DSP. When the mute function is activated both amplifiers are disabled. In a telephone this function may be used to provide the user with a secrecy function.

The devices offer the user single supply operation and allow power consumption of 40mW typically (and only 1.25 mW typical in power down mode).

The Voice-band Audio Processor is designed to provide a direct interface to the microphone, earpiece and DSP.

The Earpiece Interface.

This interface provides a balanced output from the differential output amplifier which drives a piezo speaker without the need for additional active components.

The output amplifier has adjustable gain-setting via the external resistor network, R1 and R2. It is recommended that the value of R1+R2 is set greater than 10 kΩ to reduce loading effects on the amplifier, and less than 100 kΩ to minimise noise and distortion due to the time constant of the parallel resistor combination of R1 and R2 with the capacitance at the gain-set pin *EARGS*.

The output stage may be disabled by using the earphone mute control function. This prevents the audio signal from being sent to the earphone and allows a secrecy function to be incorporated in the system.

The Microphone Interface.

A direct interface is provided to an electret type microphone. The reference voltage for the microphone amplifier and the bias voltage for the electret microphone are generated on-chip. Thus minimising the external circuitry around the device.

When the input amplifier is disabled the device transmits only zero codes.

In the linear mode of operation the microphone interface provides an adjustable volume control, this provides the user with a "soft touch" volume facility. The data word is 16 bits long. The first 13 bits contain the linear data and bits 13-15 allow the volume level to be adjusted in 8 steps between -18 dBm0 and +3 dBm0. In the companded mode of operation the data is transmitted and received in 8-bit words. The mode of operation is pin selectable. Use of the linear mode simplifies software in the DSP.

The DSP Interface.

The Voice-band audio processor provides a standard serial interface to a TMS320 DSP or any other standard DSP. Transmit and receive directions can be operated independently.

The distinguishing features between the different devices in Texas Instruments family of VBAPs are the frequency of the master clock, the out-of-band rejection characteristics of the filters, the companded format of the digital data and the minimum supply voltage at which they operate. The devices are tailored for use in cordless and cellular telephones in particular AMPS/TACS, CT-2 and GSM systems. Although targeted at these areas the devices are suitable for use in many voice-band data acquisition applications using a DSP; for example, digital encryption, digital voice-band, data storage, instrumentation and ATE.

2.4 VBAPs in Mobile Phones

Though suitable for a wide range of voice band applications using DSP such as digital encryption, data storage, portable instrumentation and answering machines, the prime application for VBAPs is undoubtedly mobile phones. In fact the whole range of Texas Instruments' VBAPs has been tailored for use in cordless and cellular telephones; in particular AMPS/TACS, CT-2 and GSM systems.

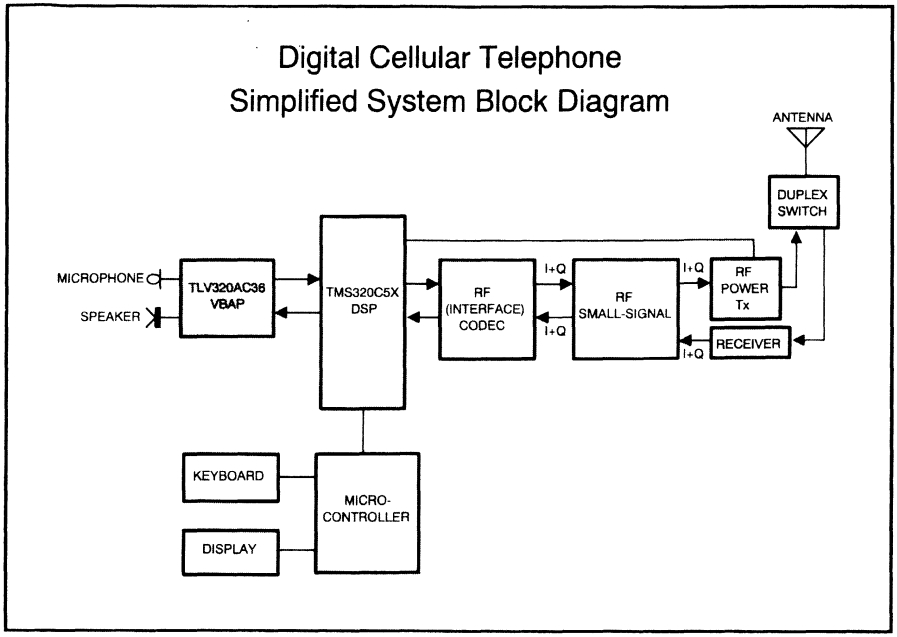


Figure 2.5 - Digital Mobile Phone - Simplified System Block Diagram

Figure 2.5 shows a simplified block diagram of a digital mobile phone which uses the VBAP to minimise the number of ICs and external passive components needed to implement the voice-band section of the phone.

The VBAP family, shown in Figure 2.7, is also available in 20 pin dual-in-line or wide body small-outline packages. The devices are characterised from 0°C to 70°C or -40°C to 85°C.

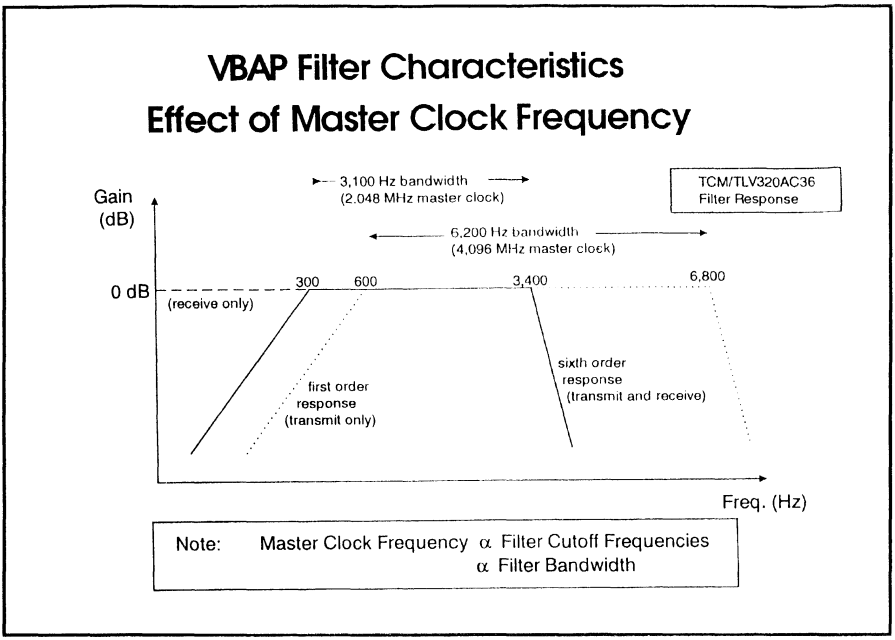


Figure 2.6 - VBAP Filter Characteristics

The various members of the product family are distinguished by the type of companding method used (μ– or A-law) and the master clock frequency which is applied to the CLK pin of the VBAP. This clock frequency has a significant effect on the filter response of the device. The cut-off frequencies of the switched capacitor filters are directly proportional to the master clock frequency. This has the overall effect that the bandwidth of the VBAP is also directly proportional to the master clock frequency. For example, in the case of the TCM/TLV320AC36 types of VBAP, the application of 4.096 MHz to the CLK pin produces a bandwidth which is twice that produced by the standard 2.048 Mhz master clock. This is illustrated in figure 2.6.

Each member of the family of VBAPs has been optimised to operate at its respective master clock frequency. These clock frequencies produce filter characteristics which are compatable with voice band signals. However the VBAP is useble, with some performance degradation, up to bandwidths of 10 kHz by increasing the standard clock frequency of 2.048, in the case of the TCM/TLV320AC36 types, by a factor of approximately 3.

Voice Band Audio Processors

Product Range and Features

Device Name	Supply Voltage (V)	μ or A Law	Master Clock (MHz)	Primary Application	Comment
TCM320AC36	+5	μ	2.048	Generic	Most Common Freq for
TCM320AC37	+5	A	2.048	Generic	Personal Comms.
(TCM320AC38)	+5	μ	2.6	GSM	All GSM have this
TCM320AC39	+5	A	2.6	GSM	frequency
(TCM320AC40)	+5	μ	1.152	DECT	All DECT have this
(TCM320AC41)	+5	A	1.152	DECT	frequency
(TCM320AC42)	+5	μ	1.944	USDC	All USDC have this
(TCM320AC43)	+5	A	1.944	USDC	frequency
(TCM320AC44)	+5	μ	1.536	Wireless PABX	Standard COMBO Central
(TCM320AC45)	+5	A	1.536	Wireless PABX	Office Frequency
TCM320AC46	+5	μ	2.048	Generic	Lower cost versions
(TCM320AC47)	+5	A	2.048	Generic	of 36/37
TCM320AC56	+5	μ	2.048	Generic	Versions of 36/37 without
(TCM320AC57)	+5	A	2.048	Generic	bit squelch
TLV320AC36	+3	μ	2.048		3-Volt version of 36

Note: Type Numbers in Parentheses not yet available

Figure 2.7 - The VBAP Product Family.

Figure 2.7 shows the growing range of voice band audio processors and indicates some of the principle features and applications of the various devices. Each device type is targetted at a particular subset of the mobile communications market. This ranges from the specific needs of systems such as GSM (Group Speciale Mobile) to more generic applications in analog cellular phones.

3 Audio Bandwidth AICs

3.1 Introduction

Signal bandwidth capability is one of the main criteria by which a designer selects an analog interface circuit. The VBAP devices discussed previously could handle bandwidths up to approximately 3 kHz only. The next part of our discussion deals with AICs which can process audio bandwidth signals; that is signals up to approximately 20 kHz.

As performance requirements get higher, so the need to use alternative circuit techniques and architectures becomes necessary. Before looking at the individual devices in more detail it is worth reviewing some the fundamental aspects of sampling theory which will help to explain the some of the design philosopies used and assist in getting the best performance out of these products in real applications.

3.2 Sampling and Quantisation

In order to produce a discrete digital representation of a continuously varying analog signal, it is necessary to take samples of the signal at regular intervals and convert them from analog into digital form. In an ideal situation the sampling function is a train of impulses, each of which are infinitessimally narrow and have unit area. The frequency of these pulses is the sampling rate (fs). The input signal can also be idealised by considering it to be truly band limited, containing no components in its spectrum above a certain frequency.

The ideal sampling condition, represented in both the frequency and time domains, is shown in figure 2.8. The effet of sampling in the time domain is to produce an amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectrum of the input signal with that of the pulse train to produce the combined spectrum shown, with double sidebands around each discrete frequency which are produced by the amplitude modulation. In effect some of the higher frequencies are "folded back" so that they produce interference at lower ones. This interference causes distortion which is called aliasing. Aliases cannot be removed by subsequent processing.

If we assume that the input signal is band limited to a frequency f1 and is sampled at frequency fs it is clear it is clear from figure 2.7 that the overlap (and hence aliasing) will not occur if

$$f1 < fs - f1$$

otherwise written as : $2f1 < fs$

This is a simple statement of Nyquist's sampling theory.

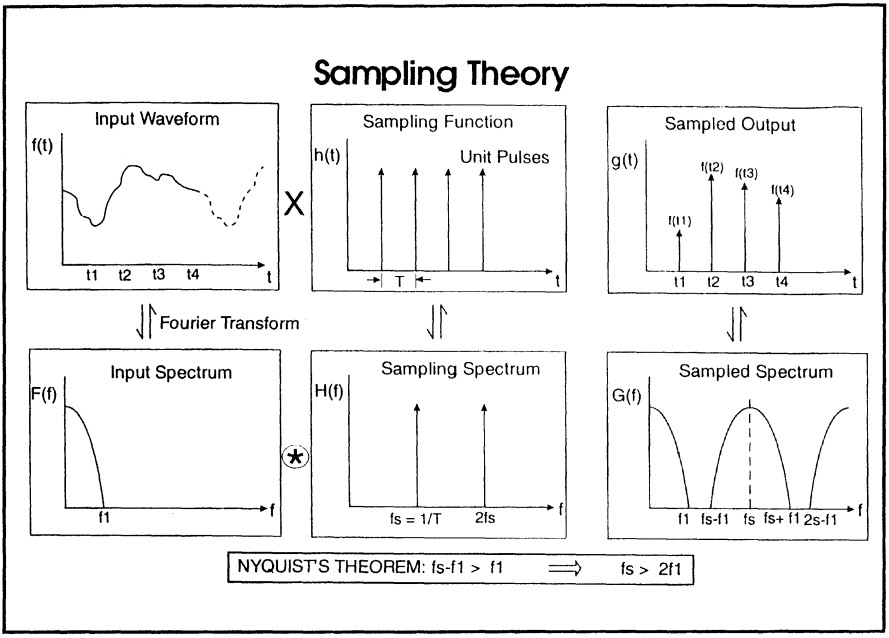


Figure 2.8 - Time Domain and Frequency Domain Aspects of Sampling (Ideal Case)

Therefore, if sampling is done at a frequency at least twice as great as the maximum frequency of the input signal, no aliasing will occur and all the signal information can be extracted. This is Nyquist's Sampling Theorem which provides a basic criterion for the selection of the sampling rate required by the convertre to process an input signal of a given bandwidth.

In real sampling, however, the width of each sample is finite and this gives rise to a modulation error of (sin x) / x. This error can be digitally compensated for prior to reconversion of the samples back into digital form.

The other important fact to remember is that a real signal is not completely band limited. The outer edges of the input signal spectra, though low in amplitude, will be aliased back into the band of interest. To avoid the possibility of this alias interfering adversely with the system performance two solutions are possible. The first is to increase the sample rate so that less of the alias appears in band. The second is to add an anti-alias filter in the signal path prior to the samplig stage. This band limits the input signal and ensures that any resultant aliases are well below the level at which they might aversely affect the signal. Increasing the sample rate will often require that a faster ADC is used which is expensive. Consequently the addition of an anti-aliasing filter is often the most cost effective method of avoiding the effects of aliasing. Sometimes a combination of increased sampling rate and anti-aliasing filter is chosen to optimise performance.

Quantisation refers to the discrete nature of digitally represented signals. Because a continuously variable analog signal has been replaced by a non-continuous series of

digital code, a certain amount of information has been lost and distortion has been introduced into the new representation of the original signal. This is called quantisation noise.

3.3 Oversampling

An ADC which is sampling an input signal at the Nyquist rate (twice the maximum input bandwidth) will produce a quantisation noise, or error, of $q / (12)^{1/2}$ (where q is the width of one step of the converter) within the signal band of f/2. This is illustrated in figure 2.9. Comparing this quantisation noise with the amplitude of a sinewave input we find that the theoretical signal to noise ratio (SNR) is given by the expression

$$\text{Theoretical SNR} = 6.02n + 1.76\ \text{dB}$$

where n is the resolution of the ADC.

For example, the SNR of a 12 bit ADC has a theoretical upper limit of 74 dB.

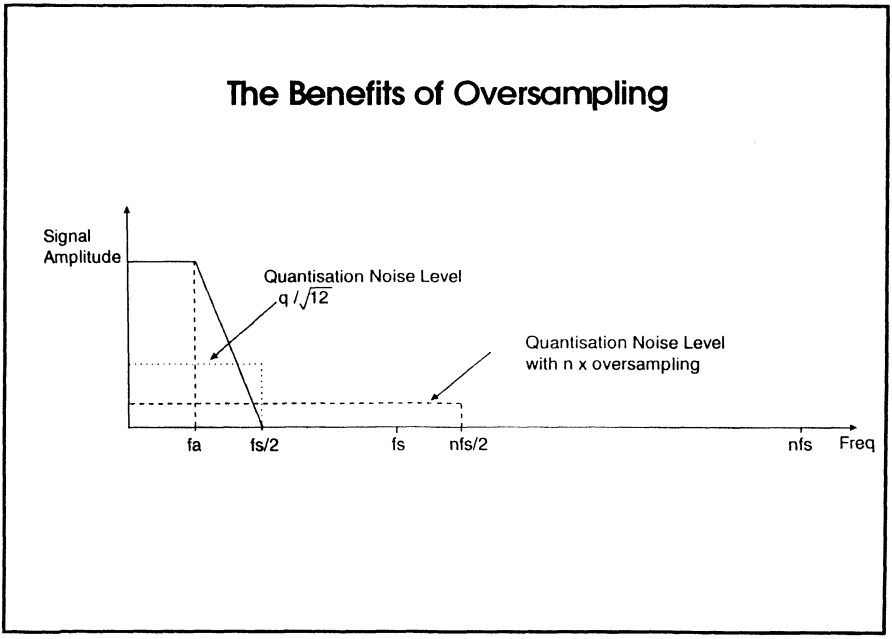


Figure 2.9 - The Benefits of Oversampling

Using the same equation we find that the theoretical SNR of a 1-bit ADC, sampling at the Nyquist rate, fs (2 x maximum input frequency of interest) is (somewhat surprisingly) as high as 7.78 dB !

If we now increase the sampling rate from fs to some multiple, nfs, we find that the same total amount of quantisation noise is spread over a wider bandwidth, nfs/2 as shown in figure 2.9. This has the effect of reducing the amount of noise in the signal band of interest. The quantisation noise which now appears outside of the signal band can be filtered out . This has the overall effect of increasing the resultant SNR in the band of interest. Here then is the basis of oversampling. The benefits of oversampling are used to produce excellent performance in sigma-delta converters.

3.4 Sigma-Delta Analog-to-Digital Converters

The earliest laboratory developments in sigma-delta converters (otherwise known as delta-sigma converters) began several years ago. However the commercial potential of these devices did not get become available until relatively recently when high speed digital and analog integrated circuit capability began to merge in either single processes or pairs of extremely compatible separate processes.

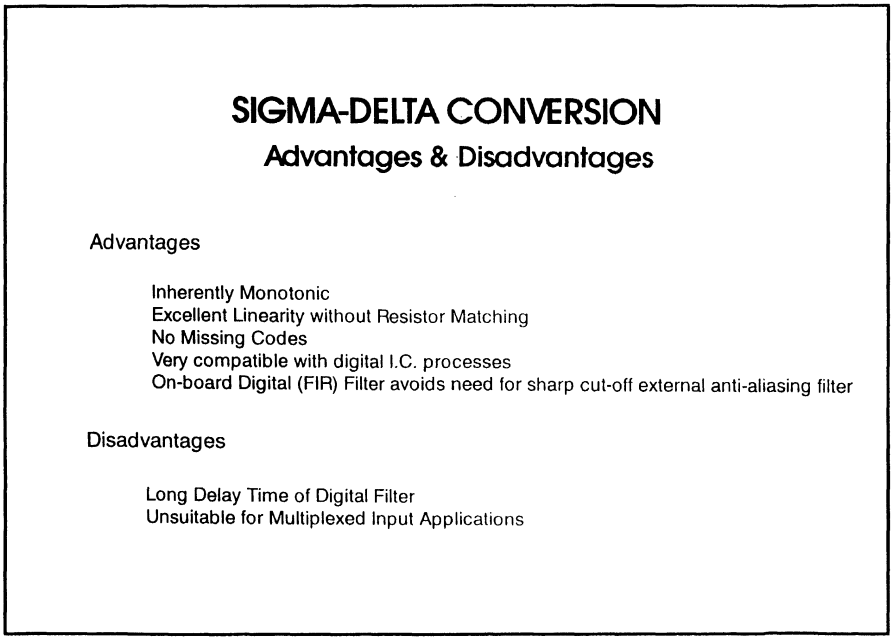


Figure 2.10 - Advantages and Disadvantages of Sigma-Delta Converters

Sigma-Delta converters have several advantages over alternative types of converter although they do have a few disdavantages also. These are reviewed in figure 2.10.

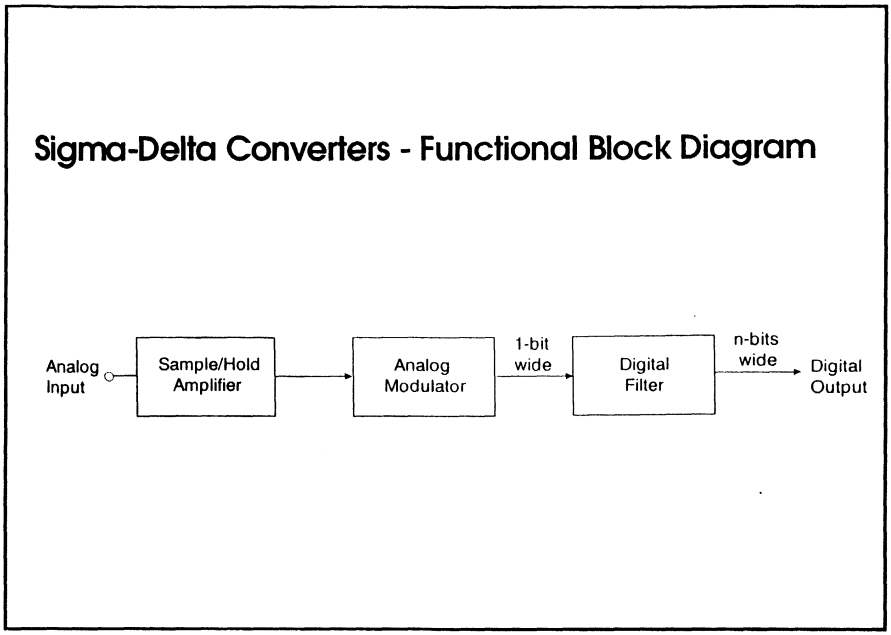


Figure 2.11 - Sigma-Delta Converter - Functional Block Diagram

The simplified structure of a sigma-delta ADC is shown in figure 2.11. The signal is first applied to the input of a coarse sample/hold stage which steadies the input during susequent bit conversions. It is then passed on to the analog modulator which converts the analog signal into a serial bit stream.

The serial digital output from the analog modulator is then processed by a digital filter which produces an average value of the data over several clock periods. Frequencies of maximum noise rejection occur at fs/N, 2fs/N, 3fs/N etc. where N is the number of samples in each average and fs is the sampling rate. Both N and fs can be selected to produce maximum noise rejection at useful frequencies such as 50 Hz and 60 Hz.

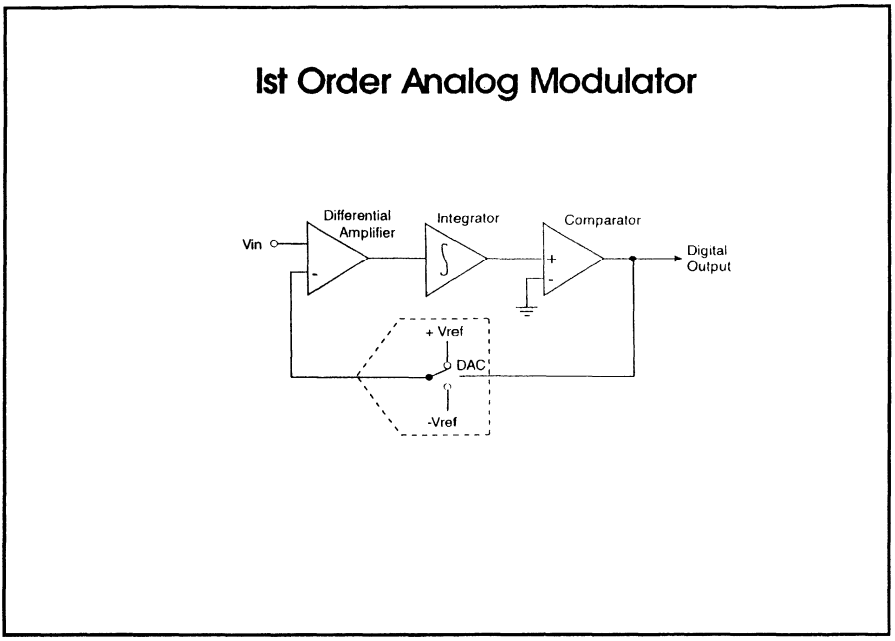


Figure 2.12 - 1st Order Analog Modulator

The actual analog to digital conversion process is performed by the analog modulator. In its simplest form this consists of a differential amplifier, single integrator, comparator and 1-bit DAC connected in a closed loop configuration as shown in figure 2.12 which illustrates a 1st Order modulator. Athough continous time circuit techniques are implied in figure 2.12, switched capacitor methods are typically used at the IC level to implement the modulator structure. The analog modulator converts the analog input signal into a 1-bit wide serial digital output. A timing circuit is often included at the output of the modulator which synchronises its operation.

The modulator also shapes the quantisation noise within the signal frequency band. This has the effect of pushing a significant percentage of the quantisation noise out of the signal band where it can be filtered by the digital filter.

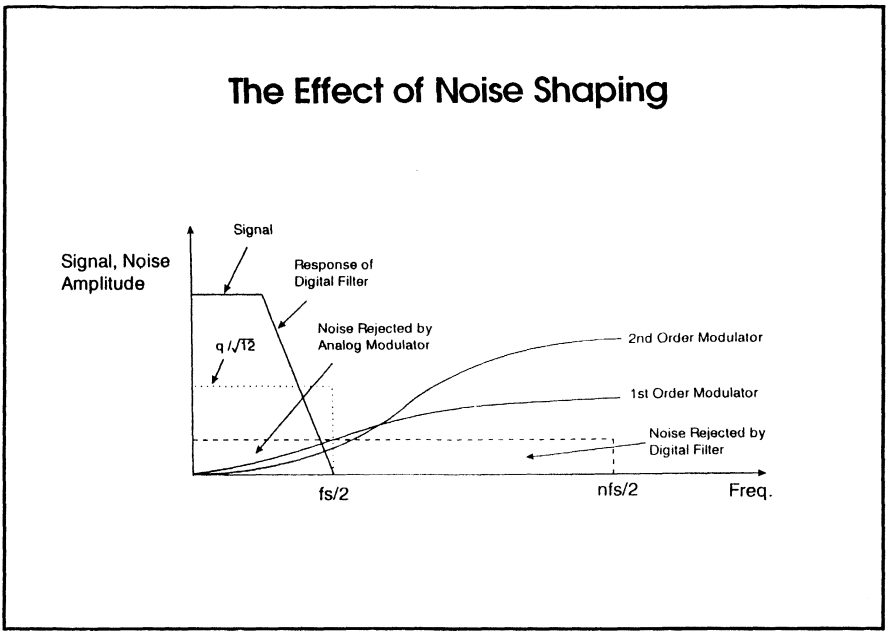


Figure 2.13 - The Effect of Noise Shaping

The number of integrators which are included determines the order of the modulator. The higher the order of the modulator the greater the amount of quantisation noise which is pushed out of band. Higher order analog modulators enable increased resolution converters offering enhanced single to noise ratios to be produced without needing to increase the oversampling rate. The effect of noise shaping produced by 1st and 2nd order modulators is shown in figure 2.13.

The idea of increasing the order of the modulator to a high number sufficient to achieve the any desired resolution and SNR is an attractive one. Unfortuneately there is rarely gain without some pain. Higher order modulators tend to be more difficult to stabilise. Most sigma-delta converters tend to use modulators which are 5th order or less.

3.5 TLC320AD55 Sigma-Delta AIC

TLC320AD55 - Sigma-Delta AIC

Features

- Single 5V Power Supply
- 89 dB Dynamic Range
- Serial Port Interface
- 14/16 bit Resolution
- Anti-aliasing and Anti-imaging Filters
- Differential architecture
- Internal reference voltage (Vref)
- Internal 64X oversampling
- Power down mode (to 1 mW)
- 80 dB SNR
- Phone mode output control
- 2's complement format
- Programmable conversion rate
  = MCLK/ (Fk x 256) , Fk = 1,2,3,....256
- System test modes
  - Digital loopback test
  - Analog loopback test

Applications

- V.34 Modems
- DSP Analog Interface
- Noise Cancellation
- Speech Processing
- Industrial Process Control

Figure 2.14 - TLC320AD55 Features and Applications

The TLC320AD55 is a sigma-delta AIC which offers up to 16 bit resolution and in excess of 90 dB SNR. Its principle features are shown in figure 2.14.

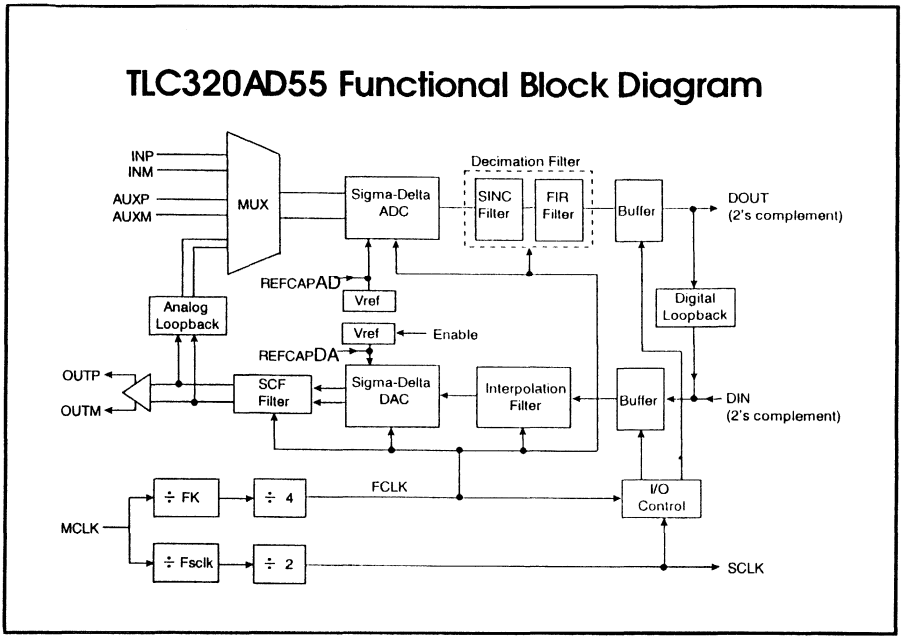


Figure 2.15 - TLC320AD55 Functional Block Diagram

It includes a 4th order analog modulator and uses a differential architecture for the analog signal path as shown in figure 2.15. This helps to reduce common mode noise and distortion effects and significantly enhances the IC's dynamic performance.

The TLC320AD55 includes separate on-board references for the ADC and DAC portions of the device. The timing of the internal logic is derived from an external master clock applied to the device at the MCLK pin. An analog input multiplexer is included which allows signals from either the main input or an auxiliary channel to be processed.

In self-test mode the multiplexer channel can be selected to accept inputs from the DAC output.

The TLC320AD55 operates at 64x oversampling rate. This simplifies any external anti-aliasing filters which are needed to be included in the input signal path prior to the input of the ADC. In fact a single pole low pass filter is normally sufficient for this task. the TLC320AD55 interfaces readily to a wide range of Digital Signal Processors (DSPs) including the industry standard TMS320 family.

V.34 Modem Characteristics

Maximum Data Rate	28,800 bits/sec on GSTN
Many Data Signalling Rates Supported	2,400 - 28,800 in multiples of 2,400
Probing Tone at Start of Connection	Allows two V.34 Modems to adjust themselves to each other and to the characteristics of the line to provide the highest possible data transmission rate
Auxiliary Channel	200 bits/sec
QAM Modulation	Uses 960 point constellation
Transmit Pre-emphasis Filter	Filter Characteristics selected by remote modem to compensate for amplitude distortion

Figure 2.16 - V.34 Modem Characteristics

This high performance sigma-delta AIC is suitable for a wide range of applications including noise cancellation and speech processing. However it was designed specifically to meet the performance demands of V.34 modems. Previously dubbed V Fast, the V.34 specification has now been formally adopted by the ITU. Some of the more important features of this standard are shown in figure 2.16.

The V.34 modem can transmit and receive data at a maximum rate of 28.8 kBits per second over the general switched telephone network (GSTN). This is achieved by a combination of quadrature amplitude modulation (QAM) and trellis coding. The data is coded into any one of 960 points on a QAM superconstellation. A high degree of "intelligence" has been incorporated into this modem standard. For example the carrier frequency to be used is determined during the start-up phase of the modem. This will be influenced by the bandwidth characteristics of the line and the error rates measured during the start-up phase. During this phase a complex probing tone is sent to the far end modem. The results gained from this probe are then returned from the far end. The combination of symbol rate and carrier frequency are then selected to match the quality of the line and the modems connected to it.

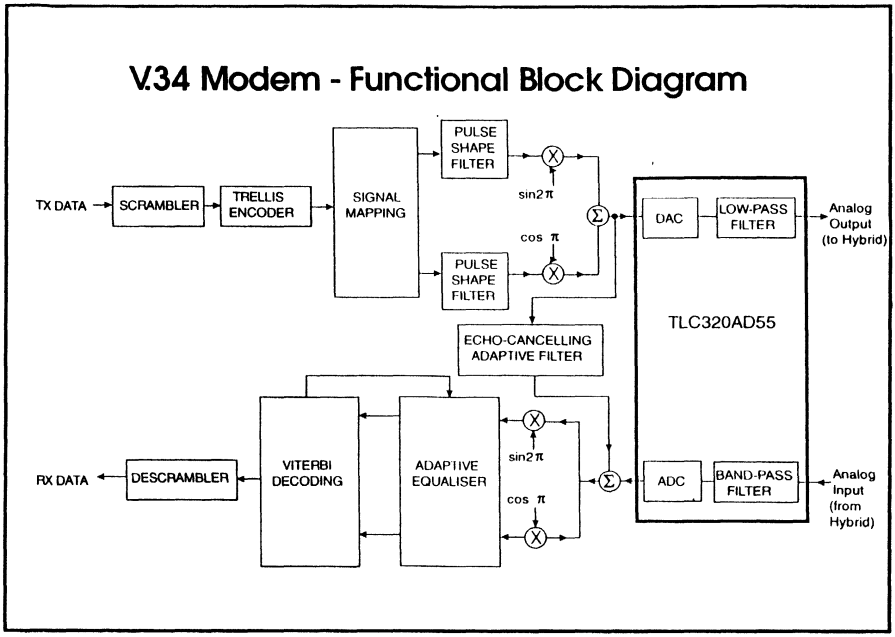


Figure 2.17 - V.34 Functional Block Diagram

Other features of the V.34 modem include full duplex or half duplex operation, preemphasis and auxiliary data channel. Most of the data coding and modulation is performed digitally by the DSP. However the data to be transmitted eventually has to be converted into analog form by a DAC in order to be sent over the GSTN. Conversely received analog data must be converted into digital form by an ADC in order to be processed by the DSP. The TLC320AD55 includes both these converter functions and an efficient interface to the DSP. The contribution which the TLC320AD55 makes to the analog "front-end" of the V.34 modem is illustrated in figure 2.17. The ADC, DAC, and efficient interface to the DSP are all included on the AIC. As can be seen, the majority of the signal processing is performed in the digital domain by the DSP.

4 TLC320AD55 Evaluation Board

4.1 Introduction

The next part of this section of the seminar has been supplied by John Walliker and Julian Daley of University College, London who have developed an evaluation board for the TLC320AD55.

4.1.1 Aims

The objective was to design a development board (the AD55-EVM) which would allow prospective users of the TLC320ADAD55 to determine its capabilities with a minimum of effort. The board can be directly connected to the inexpensive TMS320C5x DSP Starter Kit (DSK5x), or to any other system with a compatible synchronous serial interface. Directly compatible DSP devices include the TMS320C2x, C3x, C5x and many products from other companies. Some of the main features of the evaluation board are shown in figure 2.18

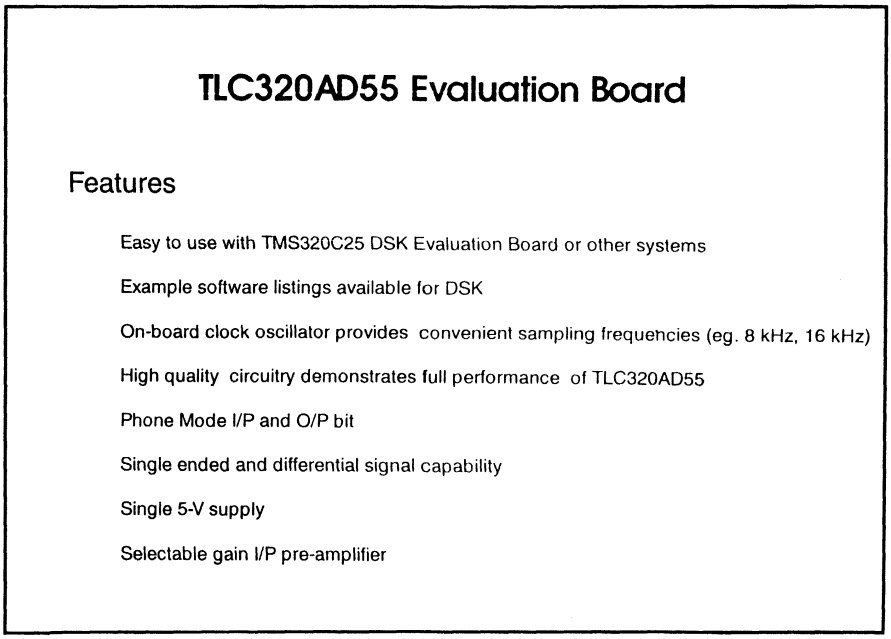


Figure 2.18 - The TLC320AD55 Evaluation Board Features

Example programs are provided for the DSK5x development system which allow the board to be used as a sine or sawtooth waveform generator, or to output on the DAC samples read in from the ADC. In this echo mode signal processing functions such as filtering can also be carried out.

The evaluation board was also interfaced to a Loughborough Sound Images TMS320C25 development board and this was used to transfer analogue data to a personal computer running real-time FFT spectrum analysis software. This system was used to prepare the ADC and DAC spectrograms shown in this seminar.

4.1.2 Overview AD55-EVM Evaluation Board

The TLC320AD55 is a sigma-delta AIC with many features that make it suitable for DSP based applications

Single 5-V supply

Better than 80dB signal to noise

Software programmable sampling rate

Serial interface

Small package size

The AD55-EVM was designed to demonstrate the advantages of the TLC320AD55 for DSP based applications.

Figure 2.19 shows a block diagram of AD55-EVM. The input signal is first buffered and optionally amplified by the preamp stage before being level shifted and converted to a differential pair of signals. The anti-aliasing filter is a simple continuous time filter to remove rf noise. The output from the codec is converted to a single ended signal and is filtered to remove noise generated by the codecs switched capacitor reconstruction filter.

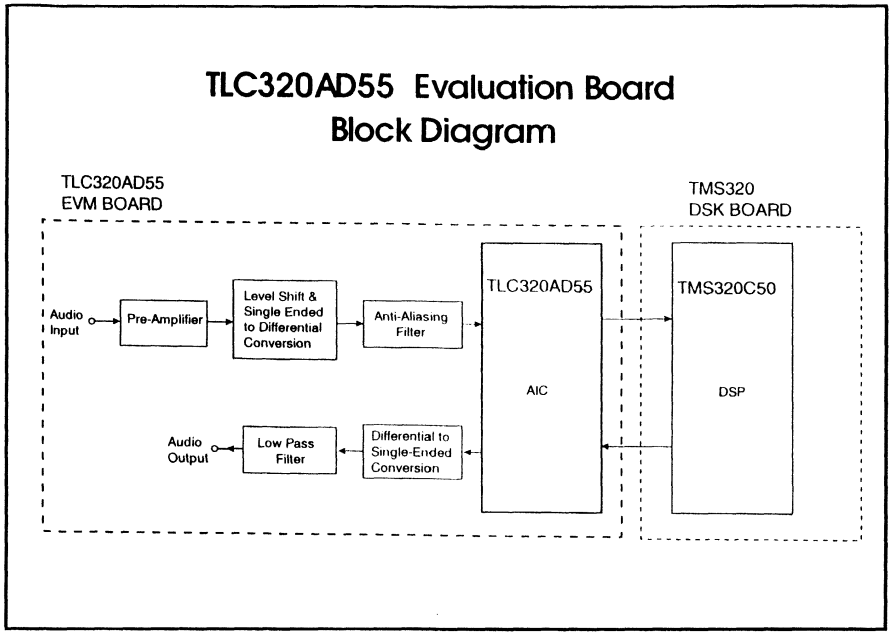


Figure 2.19 - TLC320AD55 Evaluation Board Block Diagram

A negative power supply is generated on the AD55-EVM to allow for dc coupled input and output signals. The clock signal for the codec can be generated by an oscillator on the board, or from an external clock. The TMC320AD55C is reset by decoding a block of I/O addresses.

4.1.3 Special considerations when using sigma-delta converters.

Sigma-delta analogue-to-digital converters consist of a 1-bit ADC (a comparator) combined with a high order modulator (fourth order in the case of the AD55) and digital filters in a feedback system. The ADC is clocked much faster than the desired output sampling frequency, (usually 64 times) and the large amount of quantisation noise generated is uniformly spread over a wide range of frequencies. A noise shaping filter reduces the noise in the passband, increasing it elsewhere. A low-pass filter then removes the unwanted high frequency quantisation noise and the signal is resampled at the desired output frequency.

Sigma-delta converters have some practical differences to other types of ADC, some generally advantageous, some not so.

Advantages:

The technique is inherently linear because there is no reference resistor chain as for example in flash or successive approximation converters. This results in extremely low distortion, which can easily be dominated by that of associated op-amps. Non-monotonicity does not occur with sigma-delta converters *and there are no missing codes.*

The digital filter which forms an integral part of the ADC is of the finite impulse response type which gives a linear phase response to the AD55. This filter avoids the need to provide a sharp cutoff anti-aliasing filter external to the AD55. However, a simple RC filter is needed to remove noise at the oversampling frequency and its multiples, where there are windows of full sensitivity with width ± Fsamp/2. If ceramic capacitors are used for this filter they should be of the COG or NPO dielectric type. Significant distortion can be introduced by the voltage dependent capacitance of other types of dielectric.

Disadvantages:

The digital filter has a relatively long time delay of about 15 samples which corresponds to 1.9 ms when operated at 8 k samples per second. This makes the device unsuitable for some control applications where this delay could cause system instability.

It is not practical to multiplex several inputs to one AD55 except at very low rates, because each channel would be corrupted by the earlier samples from other channels still propagating through the filter. In particular, note that although the AD55 has an input multiplexer this is only for selecting one or another input, not for interleaving two input channels onto one data stream.

The AD55 is optimised for AC signals and a small dc offset may be present.

4.1.4 Board Construction

The AD55-EVM printed circuit board is of a 4 layer construction with ground and power planes. This minimises the coupling of rf noise into the system by providing very low impedance to power and ground, and by shielding signal tracks. The AD55 is available in two surface-mount packages, the DW and DGG. Both have a similar footprint size, but the DGG is much thinner (only 1.2 mm high) and has 64 pins at a pitch of 0.5 mm, making it very suitable for PCMCIA and other miniature applications, but extremely difficult to hand solder. For prototype evaluation, we would strongly advise using the DW package, which only has 28 pins at a pitch of 0.05 inch and so is much easier to handle. We used surface-mounted components except for the connectors which are more robust when through-the-board mounted.

The printed circuit board is the same size as the DSK board. The AD55-EVM and the DSK can be stacked one above the other using inter-board links. The DSK should be on top, because its smoothing capacitors are relatively tall and also to improve access to the XDS510 emulator connector. If access to the top side of the AD55-EVM board is needed, for example to probe the circuit with an oscilloscope, then the boards can be placed side-by-side and interconnected using insulation displacement connectors and ribbon cable. Ribbon cables should be as short as possible, preferably less than 10cm .

A separate connector has been provided for interfacing to systems other than the DSK. This brings out the SCLK, FS\, DIN, DOUT and RESET\ signals. Each signal is interleaved with a ground conductor in the ribbon cable, allowing a longer cable length without crosstalk. Nevertheless, this cable should be as short as reasonably possible since ringing in the unterminated cable may become excessive for lengths greater than about 0.5m. This connector must not be used simultaneously with the connections around the edge of the AD55-EVM board that are specifically intended for the DSK.

4.1.5 Power Supply

The AD55-EVM board requires only +5-Vdc; a -5-V supply for some of the op-amps is generated on the board using a CMOS '7660 charge pump phase-locked to the frame sync output of the 'AD55. This eliminates the risk of audible beats between the sampling clock and the '7660. The OSC pin of the '7660 is coupled to frame sync by a small capacitor of about 100 pF. This method allows the '7660 oscillator to free-run when there is no frame sync, ensuring that the negative power is always maintained, even when the 'AD55 is held reset. The '7660 divides the signal on the OSC pin by 2 internally, ensuring that the charge pump operates at a 50% duty cycle, even with a grossly asymmetric input such as that provided by frame sync. Not all negative supply generators contain a divider - check before using any other type!

The 9-V ac transformer currently recommended for powering the DSK is not able to supply both the DSK itself and the AD55-EVM without introducing significant supply ripple because of the relatively small 1000 uF smoothing capacitors on the DSK board. This can be overcome by either increasing the transformer voltage (ensuring that the peak voltage does not exceed the voltage rating of the capacitors and that the regulators do not overheat) or by replacing the 1000 μF smoothing capacitors on the DSK with taller but otherwise compatible 2000 μF, 25-V replacements (e.g. Philips xxxx). Both of these options may invalidate the DSK warranty. The safest solution is to use a +/-5-V dc regulated power supply and connect it to the appropriate pins on the DSK board. The circuit diagram and pinouts of the DSK are in the DSK manual.

If the AD55-EVM board is used independently, a well regulated +5Vdc supply should be connected to the power input header pins. No separate negative supply is needed.

4.2 Analog Input

4.2.1 Preamp design

This amplifier stage, illustrated in figure 2.20, allows the use of either a line level input or a low level input. With the link labeled 'GAIN' removed the preamp has unity gain from DC to approximately 20 kHz. With this link inserted the preamp gain is increased by approximately 20dB.

The signal can be ac coupled if required by removing the link labelled DC. The use of two tantalum capacitors "back-to-back" allows either a positive or negative DC voltage bias at the input.

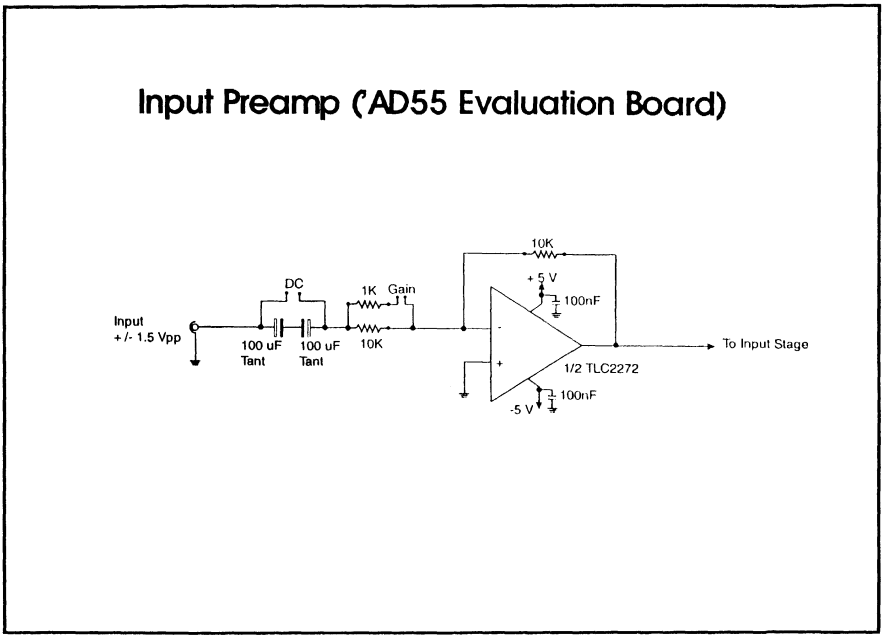


Figure 2.20 - TLC320AD55 Evaluation Board - Input Preamp

This preamp uses the op amp in the inverting configuration to ensure that the input common mode range of the op amp cannot be exceeded, since both inputs are always at a voltage close to ground. In the non-inverting configuration the op amp inputs can approach the supply rails, creating distortion.

4.2.2 Input stage design

To realise the full potential of the AD55 it is important to take care over design of the input stage. The codec uses differential inputs biased at 2.5 V and maximum code is generated for ± 1.5 V. The function of the input stage is to do the necessary level shifting and single-ended to differential conversion. There are various ways of producing the necessary signals, not all of which produce optimum results.

4.2.2.1 Design 1.

Figure 2.21 shows a simple, single op amp, single supply input stage design.

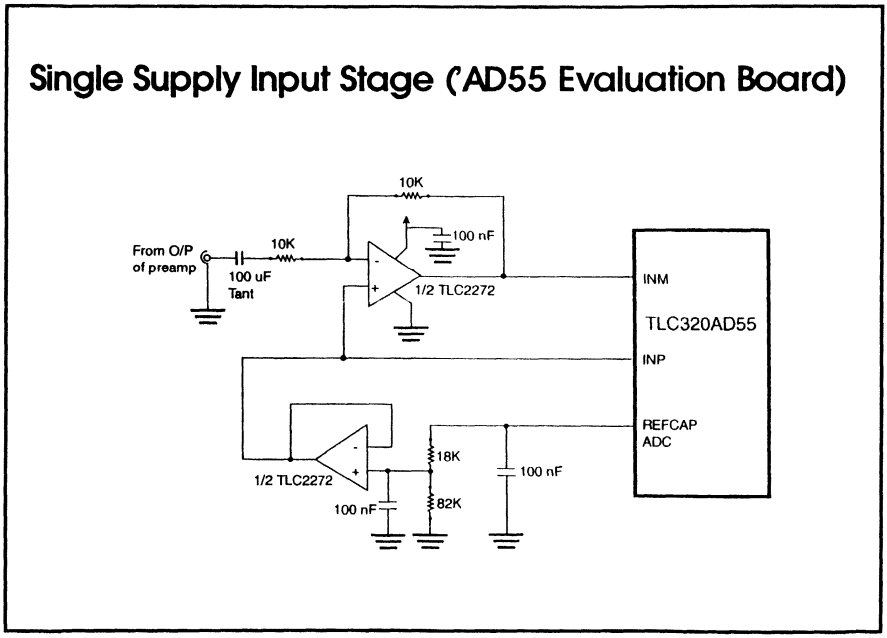


Figure 2.21 - Single Supply Input Stage (TLC320AD55 Evaluation Board)

The input signal is ac coupled by the 100 µF input capacitor and is level shifted to 2.5 V by one half the dual op amp. The other half of the op amp provides a buffered 2.5-V supply. There are some advantages to this circuit but they are outweighed by its disadvantages.

Advantages

The entire circuit can be driven from a single rail power supply

Simple design

Disadvantages

The input must be ac coupled in order to allow the level shifting required for the single supply AIC.

The TLC320AD55 has differential inputs which are desighned to provide immunity from noise and interference. To take advantage of this feature it is necessary to ensure that any noise (Δ) at the reference voltage point appears equally on both differential inputs. In this circuit the +ve input sees the noise directly whilst the -ve input sees the noise amplified by 2, giving a differential signal of $\Delta - 2\Delta = -\Delta$

Can only produce 50% of the differential voltage needed for maximum input. This effectively reduces the signal to noise ratio and dynamic range by 6dB.

Note: This design should only be used where noise performance is not an important consideration.

4.2.2.2 Design 2.

The problems with the previous design can be overcome if a negative supply is provided. Figure 2.22 shows a dual supply input stage design.

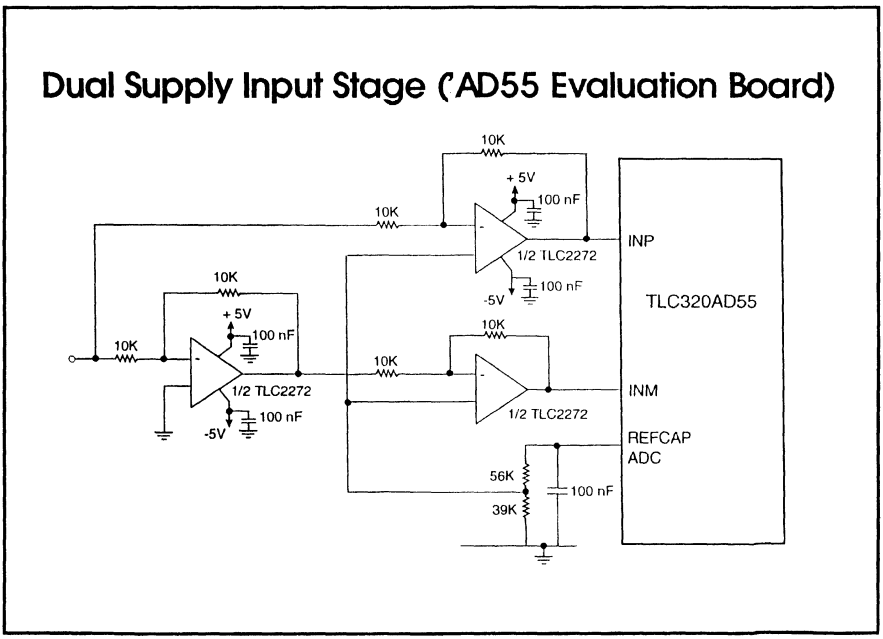


Figure 2.22 - Dual Supply Input Stage (AD55-EVM Board)

Advantages

Can be dc coupled if required to extend low frequency response.

Can produce maximum input to codec allowing full use of the device's dynamic range.

Noise on Vmid does not appear across inputs. In this design both inputs see in-phase Vmid noise of 2Δ, producing a net result of 0.

Disadvantages

Needs a negative supply

Note: This is the design of choice for maximum performance.

It is recognised that this device is likely to be used in predominantly digital designs, powered from a single +5-V supply, where the need for a negative supply could be perceived as a problem. However, since the current drawn from this negative supply will be small, it is possible to use an inverter chip to provide a local negative rail for the op amps. The 7660 device requires no external inductors and just 2 external capacitors. Its internal clock can be synchronised to the codec's sampling clock, ensuring that any noise generated by the 7660 appears on the codec's output as a DC offset rather than noise.

4.2.2.3 Op amp selection

The design of the input stage uses op amps in the inverting configuration. This has the advantage of keeping both inputs at the reference voltage, preventing problems with input common mode range.

Except for the first preamp stage, all the op amps have unity gain. This means that noise performance of most op amps is adequate. The difficult parameters to meet are output voltage range and output drive capability.

For a full scale signal the outputs of the op amps that drive the ADC inputs of the 'AD55 will reach 4.0 V. Many op amps will not behave well at this output level with a 5-V supply (in fact we tested the system at 4.75 V to allow for the minimum rated power supply voltage of the AD55).

Miniature systems often require that analogue and digital circuits are in close proximity to each other. This can lead to problems where radio frequency interference from clock signals or DSP bus lines is demodulated by opamps, leading to an increased dc offset. If the rf is modulated, then that modulation may appear at the op amp output. CMOS and BiFET opamps can be more resistant to demodulating rf than bipolars, but if this is likely to be a problem then you should evaluate the devices you plan to use. Take particular care to keep digital signals away from analogue ones, and be generous with power supply decoupling and filtering. Power planes help a great deal in reducing system noise.

The anti-aliasing filter presents a significant capacitive load which many op amps will not drive without slew-rate limiting, causing distortion of high amplitude high frequency signals.

The authors chose the TI device TLC2272 which is a LinCMOS dual op amp designed for single supply operation. It has full rail to rail output swing and an adequate output drive current.

4.2.3 Anti-aliasing filter

Sigma-Delta converters have the advantage of providing anti-aliasing filtering as an integral part of their operation. However this filtering has 'holes' in it, at multiples of the oversampling frequency. The TMC320AD55C is a 64 times oversampling converter so for a sampling rate of 8 kHz the first 'hole' will be centred at 512 kHz (and will be 8 kHz wide). It is important to ensure any energy at this frequency is not present across the inputs to the codec. A simple single pole RC filter is sufficient. Two filter configurations are possible, as shown in Figure 2.23.

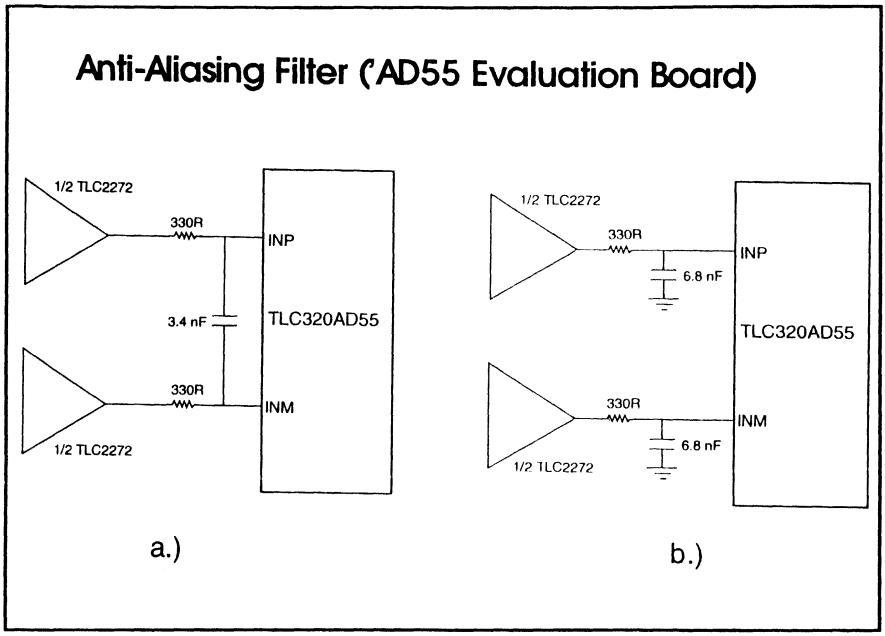


Figure 2.23 - Anti-aliasing Filter Options (AD55-EVM Evaluation Board)

Figure 2.23a gives good rejection of differential noise signals but common mode noise is not removed. Figure 2.23b gives good rejection of common mode noise signals and, if the capacitors and resistors are well matched, good rejection of differential noise.

Since most noise sources are likely to be coupled equally into both inputs the filter in Figure 2.23b is usually the best choice (the evaluation board has footprints to allow for either or both configurations).

4.2.4 ADC Results from AD55-EVM Evaluation Board

To evaluate the performance of the ADC side of the AD55-EVM two key measurements were performed. To assess signal-to-noise ratio (SNR) the true RMS value of the noise received with no input was measured. This measurement was achieved by connecting the AD55-EVM through the serial interface to a DSP development board in a PC. Data could be transferred to the PC's memory for display and measurement.

The RMS value of the noise measured in this way was 0.8 least significant bits (LSB).

The RMS value of a full amplitude sine wave is $2^{16}/(2\sqrt{2})$.

Therefore Signal to Noise Ratio = 20 * log (0.8 / 23170) = 89dB

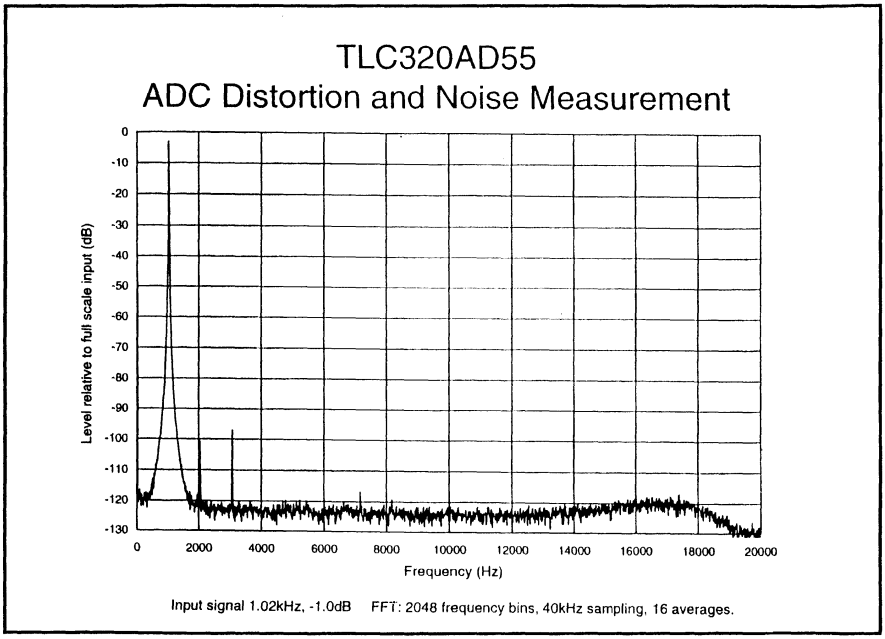


Figure 2.24 - ADC Distortion Measurement (TLC320AD55)

The second measurement is used to assess the distortion and spectral noise density of the system. Figure 2.24 shows an FFT plot obtained from the ADC of the AD55-EVM. The input signal was a 1.02-kHz sine wave at -1.0dB relative to maximum input. An HP33120A function generator was used together with a passive tuned LC filter to produce a sine wave with better than 0.001 % distortion. The FFT shows a second harmonic peak at -100dB and a 3rd harmonic peak at -95dB. The noise spectral density floor is better than 120dB below maximum for most of the pass band. The slight rise in the noise floor above 15 kHz is due to the digital noise shaping filter associated with sigma-delta converters. The noise drops off above 18 kHz due to the internal digital filter.

In summary, the AD55-EVM is an acquisition system with very low distortion and noise performance.

4.3 Analog Output

4.3.1 Differential Output Amplifier

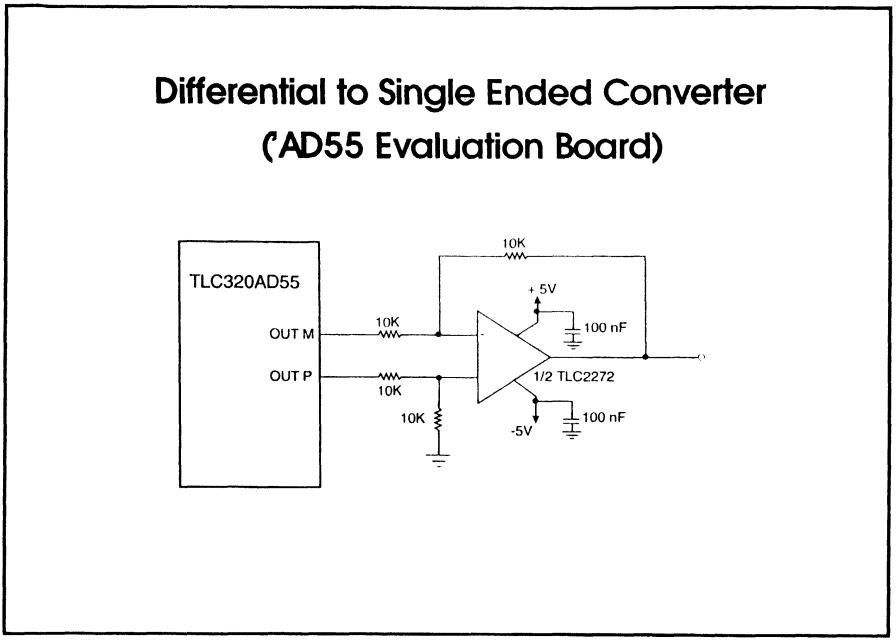


Figure 2.25 - Differential to Single-Ended Converter (AD55-EVM Evaluation Board)

The differential to single-ended converter in Figure 2.25 uses the classic differential amplifier configuration. To get good rejection of common mode noise the four resistors must be well matched. A simple way of getting good matching without having to use expensive 0.1% tolerance resistors is to use a thick film resistor pack. The absolute value of the resistors is not necessarily well specified but the resistors are generally well matched.

4.3.2 High frequency noise filter

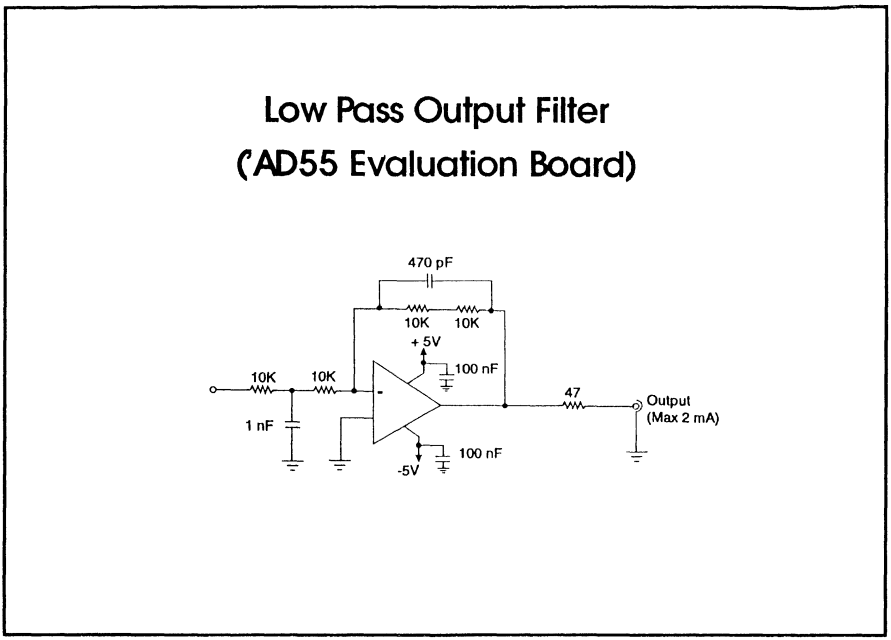


Figure 2.26 - Low Pass Output Filter (AD55-EVM Evaluation Board)

The TLC320AD55 has an internal low pass switched capacitor filter (SCF) on the output of the sigma-delta DAC. A continuous time low pass filter, connected to the analogue output of the 'AD55, is included on the evaluation board to remove high frequency noise associated with the SCF clock. The filter design, shown in figure 2.26, is a simple two stage cascaded RC network.

4.3.3 DAC Results from the AD55-EVM Evaluation Board

The DAC was characterised in its default state using a sine wave table lookup program running on a TMS320C5x DSK coupled to an AD55-EVM. This gives 10k samples per second using the 20.48 Mhz oscillator on the EVM. The DAC runs in 15-bit mode by default in order to allow secondary communication.

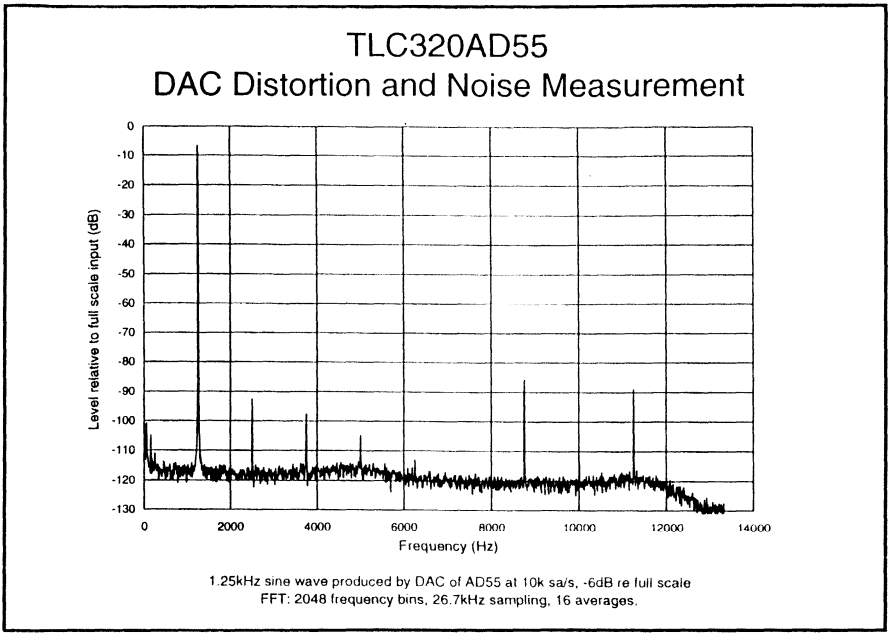


Figure 2.27 - DAC Distortion Measurement (TLC320AD55)

Figure 2.27 shows an FFT plot of the output from the AD55-EVM. This was measured using a second AD-55EVM running at 26.7 samples per second coupled to a DSP development board in a PC. This sampling frequency was chosen so as to display the first image frequencies in the output from the EVNM at 8.75 kHz and 11.25 kHz. These images are the digital-to-analog equivalent to aliases in the analog-to-digital conversion and have been attenuated by the switched capacitor reconstruction filter. There are harmonics present that may be due to rounding errors in the sine wave generation look-up table. There are some low frequency peaks in the FFT which we believe are caused by power suppy ripple.

The signal to noise and distortion are well within the specifications for the TLC320AD55.

4.4 Clocking the AD55

All timing in the AD55 is derived from the master clock input, MCLK. This is fed to two programmable dividers. One (Fk) controls the sampling and filter frequencies while the other (Fsclk) controls the serial communication speed. When the AD55 is reset, both dividers default to 8. This means that the effective sampling frequency defaults to 8.0 kHz with an MCLK of 16.384 Mhz, 10 kHz with an MCLK of 20.48 or 16.0 kHz with an MCLK of 32.768 MHz. If the required sampling frequency can be obtained using the default division ratios, then it may not be necessary to carry out any initialisation of the AIC. Otherwise, the dividers must be programmed appropriately after the 'AD55 has been reset.

If possible, the 'AD55 and its associated digital signal processor should be phase locked to the same clock. This minimises the audibility of beat signals between radio frequency noise radiated from the dsp and the sampling clock, because the beats will generally alias to dc.

Although sigma-delta converters are inherently more resistant to jitter induced noise than other types of converter the clock source should be as jitter free as possible to avoid broadening the spectrum of the input signal. The on-chip phase locked loops in DSPs can introduce significant phase jitter, possibly because of their close proximity to sources of digital noise. Therefore, if the clock for a DSP device is being generated by means of a phase-lock loop frequency multiplier, such as that in the TMS320C50, the AD55 MCLK should be driven directly by the crystal oscillator, not by the CLCKOUT1 signal from the 'C50.

If, however, the frequency multiplier is not used, and the processor clock is internally divided by two before being fed to CLKOUT1, then this signal can be used to clock the AD55 because the divider does not introduce significant jitter.

The AD55-EVM board allows several clocking options:

MODE 1 :

The 20.48 MHz crystal oscillator on the AD55 board is used to clock MCLK. This gives a default sampling frequency of 10 kHz and also allows useful sampling frequencies such as 8, 16, 20 and 40 kHz to be set using the programmable dividers. By setting jumpers on the AD55 board one can force the 'C50 in the DSK to use the 20.48 MHz clock connected to CLKIN2 in preference to the 40MHz oscillator connected to X2/CLKIN. This is done by pulling CLKMD1 high so that the 'C50 doubles the clock to 40.96 MHz. This mode should, if possible, be used when any other dsp system is interfaced to the AD55-EVM board and is recommended for most purposes.

MODE 2 :

The 40 MHz oscillator on the DSK board is divided by 2 in the 'C50 and output to CLKOUT1. This drives the 'AD55 MCLK. The default sampling frequency is 9.765625 kHz and sampling frequencies which are a whole number of kHz cannot be generated exactly. Had the DSK been provided with a 40.96 MHz oscillator, sampling frequencies of 8, 10, 16, 20 and 40 kHz would have been achieveable and this would have been the preferred mode of operation because an extra oscillator would not have been needed.

MODE 3 :

As mode 1 above, but MCLK is driven by CLKOUT1 of the 'C50. Not recommended because of the possible introduction of phase jitter into MCLK by the phase locked loop.

MODE 4 :

As mode 1, but C50 is clocked from its 40 MHz oscillator. Not recommended because of the possibility of audible beats between the clock sources.

4.5 Resetting the TLC320AD55

The TLC320AD55 is automatically reset at power-on. It can also be reset by applying a low level on the RESET\ pin or under software control by programming bit 7 of control register 1 using secondary communication. The reset signal is latched by the MCLK input and stretched internally to at least 6 MCLK cycles. Whatever the reset source, all the internal registers are set to their default values and only need to be changed if the defaults are unsuitable for the particular application.

The AD55 is held in a reset state for as long as RESET\ is low, with frame sync out high and serial clock out low. When RESET\ is released, the serial clock output begins and the falling edge of the first frame sync out occurs 46 rising serial clock edges later. There will be a further delay of 1.9 ms (at 8 kHz sample rate) associated with the digital filters within the AD55 before valid output data becomes available.

This timing is significant because of the way that the synchronous serial ports in some dsp devices such as the TMS320C50 operate. If frame sync is high when the serial port of the C50 is released from reset, a data transfer will be immediately initiated, whereas if it is low this will not happen. This is further complicated for C50s with revision 1 silicon, such as that currently supplied with the DSK5x, because the first word of data transmitted after a serial port reset with frame sync high may be random.

To prevent intermittent errors in programming the registers when using the current version of the DSK5x, it is necessary to 1) reset the 'AD55, 2) reset and release the 'C50 serial port, 3) wait for first data transfer to complete, 4) reset the 'AD55 again, 5) program any 'AD55 registers that need to be changed from the default values.

To facilitate this we have provided a programmable reset for the 'AD55 board when used in conjunction with the DSK. Address bits A1, A2, A3 and the IS\ and WR\ signals are decoded and fed to RESET\ of the 'AD55. Writing to output port zero, will therefore send a reset pulse to the 'AD55. This can, if necessary, be stretched by setting extra wait states for port zero in the wait state configuration registers of the 'C50. We were not able to use the reset method provided for the codec on the DSK5x because the BR\ signal is not brought out to a connector on the DSK

With revision 2.x or later TMS320C5x family silicon the reset input can be connected directly to the system reset, so long as all the processor initialisation is completed before the first frame sync pulse goes active low. This occurs after 46 serial clock cycles at the default sampling frequency. If this condition cannot be met, then the RESET\ input must be directly controlled by the processor. However, the double reset described above is NOT needed with rev. 2.x or higher 'C5x devices.

4.6 Serial Port Interfacing

The AD55-EVM is designed to be used in one of the following two ways and as described in section 4.1.4.

1.) A DSK5x DSP board can either be stacked on top of the AD55-EVM board using inter-board connectors, or the boards can be placed side-by-side and interconnected with short ribbon cables. Only a few ground signals are brought out from the DSK5x and very fast 'C50 clock and bus signals are transmitted between the boards. Therefore the interconnecting cables should be very short, prefereably no more than 10 cm.

2.) Alternatively, the AD55-EVM can be used in standalone mode and connected to other DSP systems such as PC plu-in development boards. A special connector is provided for this purpose which brings out the 'AD55 serial port and reset signals. Every signal is interleaved with a ground, allowing much longer ribbon cables, up to about 100 cm long, to be used reliably.

The TLC320AD55 communicates with its associated digital signal processor by means of a standard synchronous serial interface. Data transfer is controlled by the clock output from the 'AD55 which controls the operation of the serial port in the DSP. Frame synchronisation and serial data signals are sampled by the DSP on the falling edge of the clock. Each data transfer begins on the falling edge of the frame sync which remains low until all the data bits have been transmitted. It is particularly important that the clock signal is of high quality at the input to the DSP.

Two problems can occur if long interconnecting cables are used without proper termination and buffering. The first is ringing which, if severe, can exceed the logic threshold and cause incorrect clocking or even damage to the inputs of the devices. The second is excessively slow rise and fall times on the clock which can also cause spurious clocking, either because of oscillation in the input circuit of the serial port or increased susceptibility to noise. In either case the effect is that data may be clocked in on both edges of the clock, causing intermittent corruption of the transmitted and received data.

The rise and fall times of the serial clock at the paralleled transmit and receive clock inputs to the TMS320C50 on the DSK5x, when driven through 10 cm of ribbon cable, were measured. The measuremment was made with an HP5452A 2 Gigasamples per second digital oscilloscope using HP1144A 800 MHz FET probes. Thresholds of 0.8 V and 2.0 V were used, corresponding to the low and high thresholds of the 'C50. The following results were obtained.

Cable Length	t_{RISE}	t_{FALL}
10 cm	0.6 ns	2.6 ns
100 cm	1.5 ns	5.5 ns

The maximum serial clock input rise and fall times for a 40 Mhz 'C50 are :

t_{RISE} = 8 ns

t_{FALL} = 8 ns

The rise and fall time measurements for 10 cm cable were made at the 'C50 serial clock input pins on a DSK5x system while the 100 cm measurements were made at the input to a development board in a PC.

These measurements show that the serial clock quality is acceptable even with 1 metre of ribbon cable at room temeperature. However for reliable operation over the full

temperature range and in the presence of noise the cable length should be kept as short as possible.

Note that the interconnections between the DSK and the AD55-EVM contain much faster signals without interleaved grounds and should not be much longer than 10 cm.

4.7 Programming the AD55 registers

Programming the internal registers is achieved by means of secondary serial communications interleaved between the primary data transfers. A secondary transfer can be requested in one of two ways:

1. By applying a high level to the FC input pin where it is latched by the 'AD55 on the rising edge of a primary communications frame sync pulse. Although this method requires a programmable output bit it has the advantage that full 16-bit data can always be transmitted to the 'AD55 DAC. If the FC input is held continuously high, then secondary communications will be interleaved between every primary communication. This may be useful if the ALTDATA input bit is to be monitored, but it increases the software overheads by doubling the serial port interrupt rate.

2. By setting bit zero of a transmitted data word. This method is simpler because no extra hardware output bit is needed, but limits the audio data transfers to 15-bit resolution. 16-bit transfers can be selected by programming bit 0 of register 1, but once this has been done further software requests for secondary communications cannot be made, so the flag I/O signals are not accessible.

In each case, the request generates only one secondary communication immediately after the primary communication in which it was initiated.

It is important that the clock dividers are set in such a way that there is sufficient time for the secondary communications to be interleaved between primary communications. This is most easily achieved by setting the serial clock register to the same value as the sample clock register (register 4) to the same value as the sample clock register (register 3).

4.7.1 The AD55 Registers

The individual register to or from which data is to be sent is selected by a 3-bit address in bits 10, 9 and 8 of the 16 bit secondary communication. Bit 13 high selects a read cycle, low selects a write. The bottom 8 bits contain the data to be read or written.

Register 0: No Operation

This does nothing, but can be useful because it provides a means of making dummy secondary communications that don't change any registers if, for example, the FC input is hardwired high.

Register 1: Control 1

Used to select 15/16-bit output mode, analogue and digital loopback, output gain, input signal source, software powerdown and software reset. Note that once 16-bit mode has been selected it is no longer possible to make software requests for further secondary communications.

Register 2: Control 2

Used to bypass the interpolator and decimator filters, enable phone mode, set FLAG0 and FLAG1 output pin values and test for decimator FIR filter overflow. The filters should not normally be bypassed except for test purposes, or perhaps in control applications where the system delay time must be minimised at the expense of possible aliasing and a sinc(x) frequency response. The flag bits are ignored unless phone mode has been enabled.

Register 3: Fk divide

The sampling rate of the converters is MCLK / (Fk * 256). The default register value is 8 and the possible range is 0 to 255. A value of 0 is interpreted as 256. The devices we measured would sample at up to about 80 kHz, although operation at such speeds resulted in increased distortion and greatly increased dc offset.

Register 4: Fsclk divide

The serial clock frequency is MCLK / (Fsclk * 2). The default register value is 8 and the possible range is 0 to 255. A value of 0 is interpreted as 256. Normally Fsclk should be set to the same value as Fk. This will ensure that exactly one serial data transfer occurs for each sample. Other ratios between the two can result in samples being missed or multiple values being transmitted for one sample. It is also important to ensure that enough time is allowed for any secondary communications to take place if Fsclk is less than Fk. Take care also to ensure that the maximum clock speed for the DSP serial port is not exceeded. For example, if MCLK is driven from CLKOUT1 of a 'C50, then the minimum serial port cycle time of 5.2H ns is maintained so long as the contents of Fsclk is not less than 2. See section 3.3 of the TLC320AD55 data manual for a more detailed explanation.

Register 5: Control 3

The only function of the control 3 register is to disable or re-enable the DAC reference. This allows an external reference to be used instead of the on-chip one to scale the output voltage range.

(Note: H - Half Cycle Time of TMS320C50)

5 Audio Converters

5.1 Introduction

Many audio systems require either the analog-to-digital or digital-to-analog converter function but not both. Separate ADCs and DACs exist to service these applications. Some of these converters have efficient digital interfaces which give them certain similarities to the AICs discussed previously. Texas Instruments manufactures a range of separate audio converters which complement the AICs. Their main features are summarised in figure 2.28.

Analog Interface Circuit/Stereo ADC Selection Guide

Device	Configuration	Resolution (Bits)	Bandwidth (Hz)	Sample Rate (KHz)	Power Supply	Max Power Dissipation
TLC32040	Diff Input AIC	14	300-3600	19.2	+/- 5 V	430 mW
TLC32041	Diff Input AIC	14	300-3600	19.2	+/- 5 V	430 mW
TLC32044	Diff Input AIC	14	100-3800	19.2	+/- 5 V	430 mW
TLC32045	Diff Input AIC	14	100-3800	19.2	+/- 5 V	430 mW
TLC32046	Diff Input AIC	14	300-7200	25	+/- 5 V	430 mW
TLC32047	Diff Input AIC	14	300-11400	25	+/- 5 V	430 mW
TLC320AC01	Diff Input AIC	14	0-10,800	25	+ 5 V	110 mW
TLC320AC02	Diff Input AIC	14	0-10,800	25	+ 5 V	110 mW
TLC320AD55	Sigma-Delta AIC	16	0-4,000	10.3	+ 5 V	175 mW
TLC320AD57	Stereo Audio ADC	18	30-21800	48	+ 5 V	220 mW
TLC320AD58	Stereo Audio ADC	18	30-21800	48	+ 5 V	200 mW

Figure 2.28 - AIC and Audio Converter Product Range

5.2 Analog-to-Digital Converters

5.2.1 TLC320AD57 Sigma-Delta Stereo Analog-to-Digital Converter

The TLC320AD57 stereo analog-to-digital converter is specified to meet the requirements of a broad range of CD (compact disc) quality audio applications as indicated in figure 2.29. The device offers excellent dynamic performance and ease of digital interface through a single serial data output and operates from a single 5 volt supply.

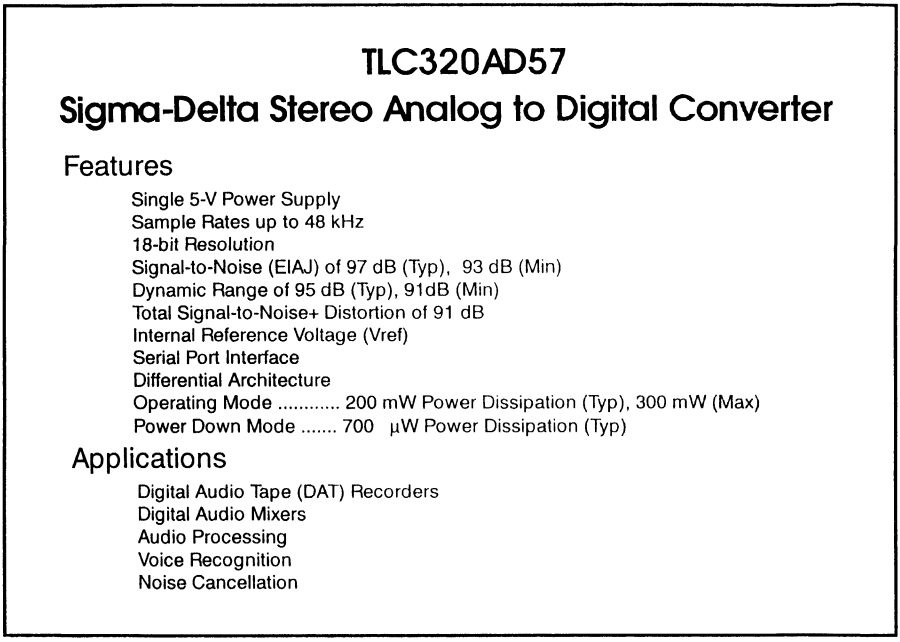


Figure 2.29 - TLC320AD57 Stereo Audio ADC - Features and Applications

Each channel of the TLC320AD57 stereo ADC contains a 64 times oversampling sigma-delta modulator as shown in figure 2.30. Each modulator is followed by a divide-by-64 decimation filter and a subsequent high pass filter which may be bypassed by asserting a high level on the HYBPyp pin of the device. Bypassing this high pass filter allows the converter to handle frequencies down to dc, should that be required.

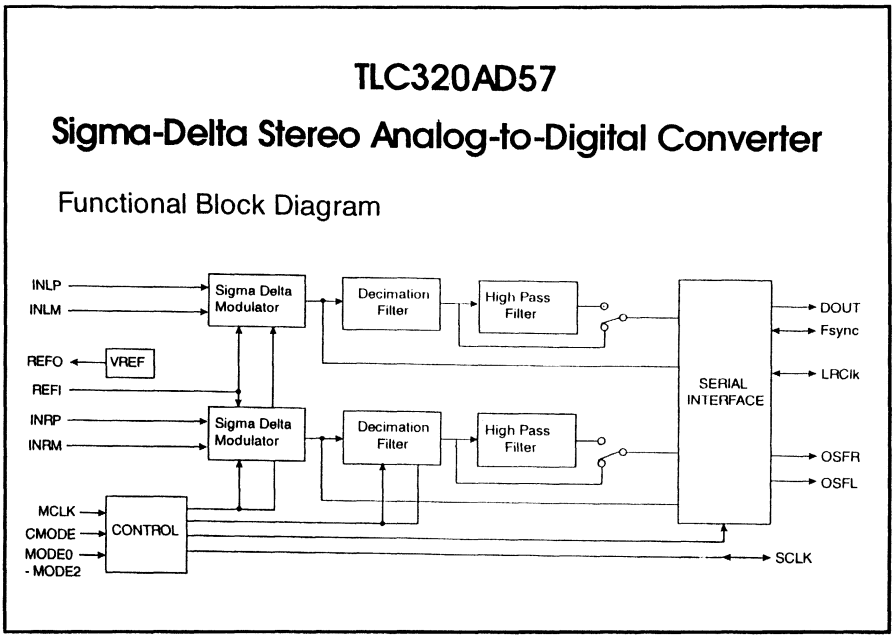


Figure 2.30 - TLC320AD57 Stereo Audio ADC - Functional Block Diagram

Both left and right channel digital conversion results are output serially from a single data output pin DOUT. The left and right channels' results can be interleaved by sequentially toggling the left/right clock pin LRClk. Left channel data is output when LRClk is high and right channel data is output when LRClk is low.

There are three slave and five master modes in which the digital interface of the TLC320AD57 can operate. As a master the device accepts a master clock input and generates LRClk, Fsync and SCLK which are provided for the synchronising of the serial port of a DSP or other control devices.

In slave modes the TLC320AD57 receives LRClk, Fsync and SCLK as inputs. The conversion cycle is synchronised to the rising edge of LRClk and the data is synchronised to the falling edge of SCLK.

The TLC320AD57 utilises a differential architecture for the internal analog signal path which yields excellent dynamic performance as indicated in figure 2.29. This includes an SNR of 97dB and total harmonic distortion of 91dB.

5.2.2 TLC320AD58 Sigma-Delta Analog-to-Digital Converter

The TLC320AD58 offers extra dynamic performance over and above that offered by the TLC320AD57 as shown in the features listed in figure 2.31.

TLC320AD58
Sigma-Delta Stereo Analog to Digital Converter

Features

Single 5-V Power Supply
Sample Rates up to 48 kHz
18-bit Resolution
Signal-to-Noise (EIAJ) of 99 dB (Typ), 95 dB (Min)
Dynamic Range of 97 dB (Typ), 93 dB (Min)
Total Signal-to-Noise+ Distortion of 95 dB (Typ)
Internal Reference Voltage (Vref)
Serial Port Interface
Differential Architecture
Operating Mode ..... 220 mW Power Dissipation (Typ), 300 mW (Max)
Power Down Mode ..... 700 μW Power Dissipation (Typ)

Applications

Digital Audio Tape (DAT) Recorders
Digital Audio Mixers
Voice Recognition
Noise Cancellation

Figure 2.31 - TLC320AD58 Features and Applications

The functional block diagram of the TLC320AD58 is shown in figure 2.32. Architecturally and functionally it is very similar to the TLC320AD57. The only significant difference is that the total gain of each channel of the TLC320AD58, though the same as that of the TLC320AD57, has been redistributed between the input stage and the high pass filter.

This change yields a useful improvement in SNR, dynamic range and total signal to noise + distortion, as indicated in figure 2.31. Also the ability to bypass the high pass filter is not available on the TLC320AD58.

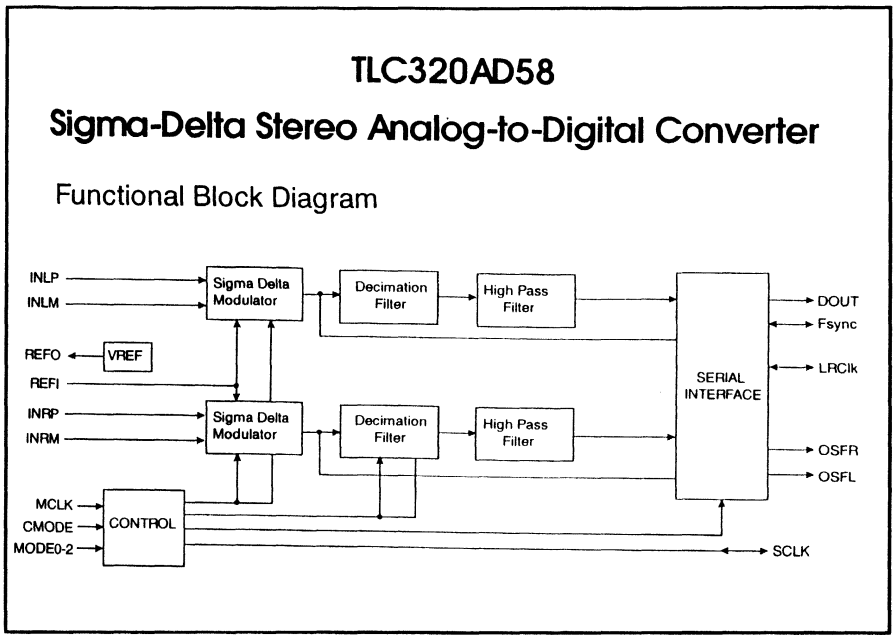


Figure 2.32 - TLC320AD58 Functional Block Diagram

5.3 PCB Layout Precaution

Several sigma-delta AICs and analog to digital converters are fabricated using separate chips for the analog and digital portions of the device. Apart from certain cost benefits which can accrue from size reductions in the digital section as finer geometry IC processes are adopted, a major improvement in signal to noise ratio can be obtained if we make use of the fact that the substrates of the two chips are separated.

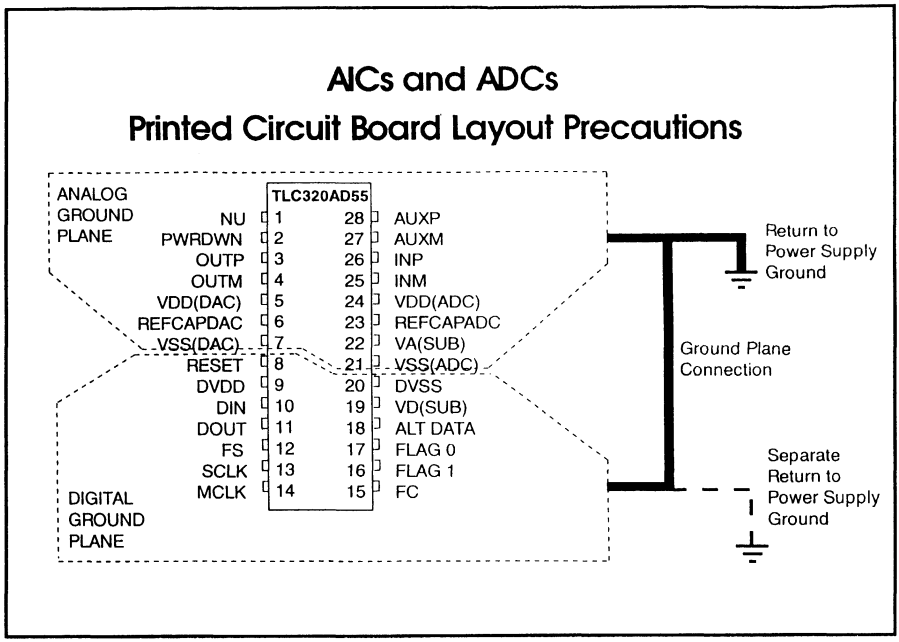


Figure 2.33 - AIC and ADC Printed Circuit Board Layout Precautions

This is achieved, as shown in figure 2.33 by keeping analog and digital portions of the printed circuit board ground plane physically apart in the area of the board immediately under the device at the boundary between the digitally related and analog related pins.

5.4 Digital-to-Analog Converters

5.4.1 TMS57014A Dual Audio Digital-to-Analog Converter

The TMS57014A uses a sigma-delta architecture to achieve a dynamic range of 96dB and a total harmonic distortion of only 0.004%. Several useful features, such as digital attenuation to -60dB and programmable de-emphasis filter, make it ideal for use in a variety of audio equipment including compact disk players and digital audio tape systems.

TMS57014A
Dual Audio Digital-to-Analog Converter

Features

- Single 5-V Power Supply
- Sample Rates(Fs) up to 48 kHz
- 18-Bit Resolution
- Pulse Width Modulation (PWM) Output
- Programmable Deemphasis Filter
  (for Sample Rates of 32, 37.8, 44.1, and 48 kHz)
- Total Harmonic Distortion of 0.004 % (Max)
- Dynamic Range of 96 dB (Min)
- Digital Attenuation to -60 dB
- Mute with Zero-Data-Detect Flags
- Serial Port Interface
- Differential Architecture
- 2's Complement Data Input

Applications

- Compact Disks
- Digital Audio Tape
- Video Cassette Recorders
- Multimedia

Figure 2.34 - TMS57014A Stereo Audio DAC - Features and Applications

Each channel contains an interpolation filter which essential adds extra data points in between those supplied to the device at the digital input. As shown in figure 3.35 the digital data then passes via the de-emphasis filter to the DAC modulator which produces a pulse width modulated signal at its differential output.

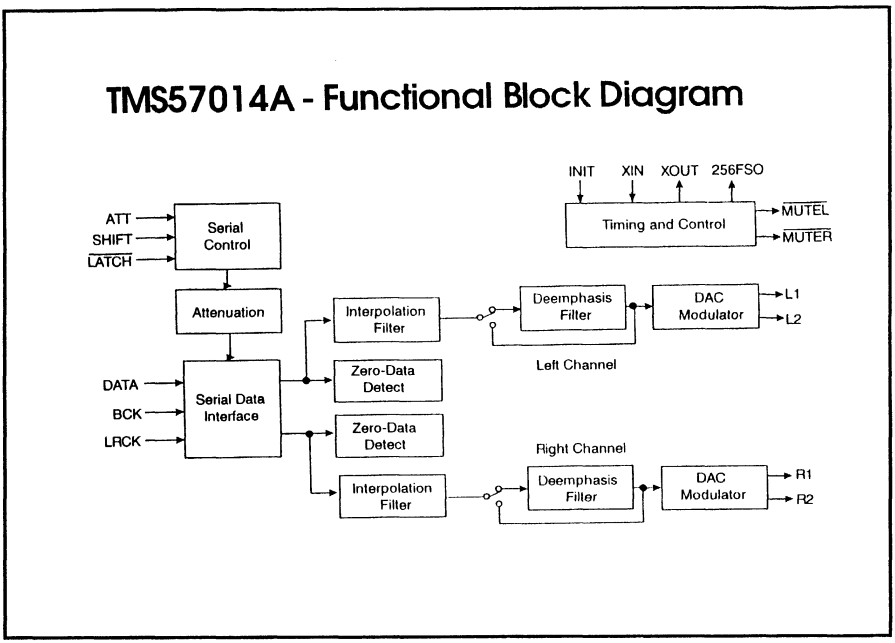


Figure 2.35 - TMS57014A Stereo Audio DAC - Functional Block Diagram

A suitable low pass filter such as that shown in figure 2.36 should be applied to the output of each DAC to convert the PWM waveform into a high quality audio signal.

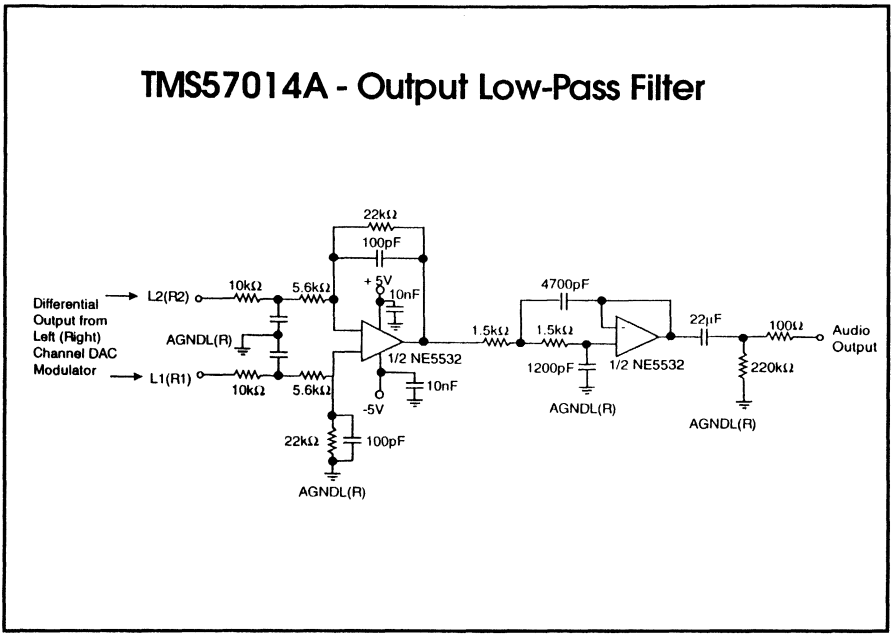


Figure 2.36 -TMS57014A Stereo Audio DAC - Output Low Pass Filter

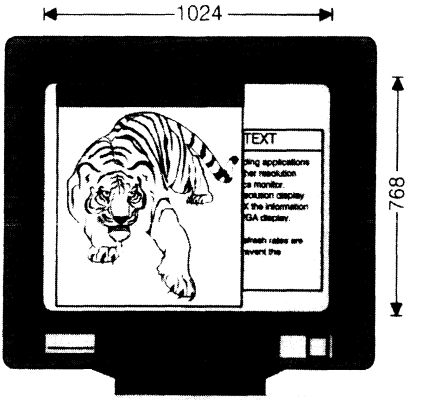
6 Video Interface Palettes

6.1 Introduction

Today's computer systems make extensive use of graphics, both in the user interface such as Windows™ and in the applications software such as desktop publications, CAD, etc.

In order to service these applications, high resolution monitors are required together with the circuits that drive them.

Introduction - Resolution and Refresh Rate



- Today's demanding applications require ever higher resolution from the graphics monitor.
- A 1024 x 768 resolution, XGA display has approx 2.5 x the information of a 640 x 480 VGA display.
- Higher screen refresh rates are demanded to prevent flicker. 72 Hz is the normal standard.
- Blanking ratio is typically 25%
- Dot clock = (No. of pixels per line) x (No. of lines per frame) x (refresh rate) x (blanking ratio)
- EG. Dot clock = 75MHz = 1024 x 768 x 72 x 1.33 or approx 129MHz at 1280 x 1024

Figure 2.37 - Video Interface Palettes - Resolution and Refresh Rates

6.1.1 Resolution and Refresh Rate

Over the years IBM VGA (Video Graphics Array), which has a resolution of 640 x 480, has dominated the overall graphics board design. However, as the technology advances, resolutions of 1024 x 768 and higher (such as 1280x1024 and 1600x1280) become the general design target.

There is also a requirement for high refresh rates, to eliminate the annoying flicker effect. The current standard is 72 Hz non-interlaced, but more designers are now

considering 76 Hz, 85 Hz and even higher. This combination of high resolution and high refresh rate demands a very fast pixel clock (dot clock).

6.2 A Video Interface Palette

A Video Interface Palette (VIP) is a complete graphics back-end on a chip. It interfaces the Video RAM of a PC or workstation with the graphics monitor. It contains a combination of fast logic functions and video DACs to transform the stored image into an analog signal for input to the monitor.

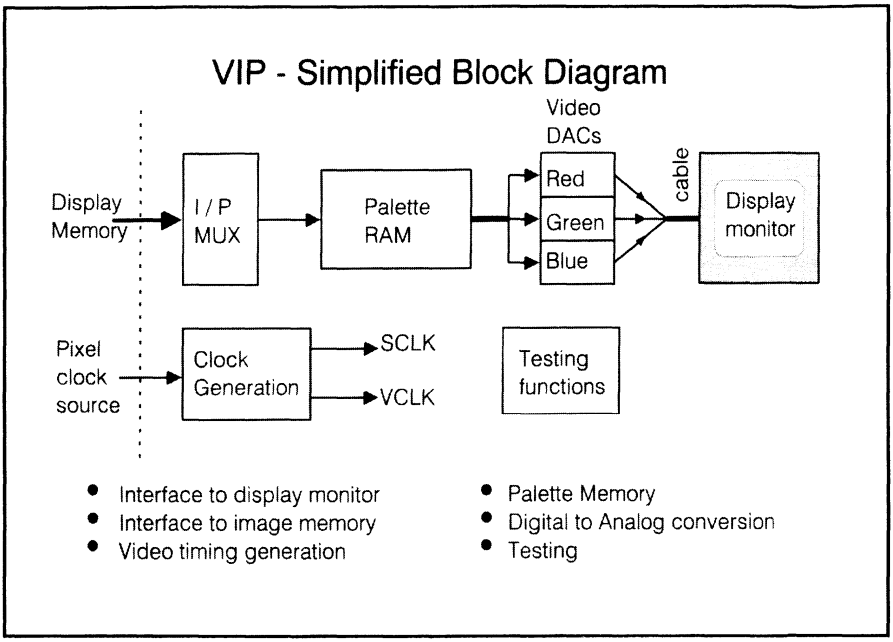


Figure 2.38 - Video Interface Palette - Simplified Block Diagram

The input multiplexer on the VIP will allow different numbers of bits-per-pixel and different numbers of pixels-per-transfer under S/W control. This, together with a programmable dot clock source allows the computer display to be set-up with different screen resolutions and numbers of colors.

In the 1, 2, 4 or 8 bits-per-pixel modes the pixel data, from the Frame Buffer goes, not to the DACs, but addresses a 256 location x 24 bit palette RAM within the VIP. This allows up to 256 colors to be resident at any one time with the 24 bits being composed of 8 bits each of red, green and blue data. The 256 colors chosen are downloaded by the host depending on the application.

The VIP also supports 16-bit and 24-bit true color modes, where the data from the Frame Buffer goes directly to the video DACs. This is usually used to present "real" images to the screen, the 24-bit mode providing "photo-realistic" images.

Because the VRAM serial port speed is limited to approximately 50 MHz, then for dot clock speeds above 50 MHz, more than 1 set of pixel data has to be transferred in each read cycle.

As more colors are demanded at higher and higher resolution then wider pixel buses are required to effect the transfer to effectively increase the bandwidth of the pixel bus.

With the advent of Windows™ 3.1 which supports 24-bit true color applications, there is an increasing demand for graphics systems which support 24-bit true color at 1024x768 resolution. As the dot-clock is approximately 80MHz at 1024x768 resolution, then 2 pixels need to be read into the VIP in each transfer. For 24-bit true color the pixel bus width would have to be 48-bits wide. In fact a 64-bit wide pixel bus is traditionally used, allowing an 8-bit overlay function.

Resolution, Colors and Frame Store Size

MIN. NUMBER OF PIXELS PER TRANSFER *	FRAME RATE	APPROX DOT CLOCK	SCREEN RESOLUTION	FRAME STORE SIZE FOR NUMBER OF COLORS (MBytes)						
1	60Hz	38MHz	800 × 600	0.25	0.5	0.5	1	1	2	2
	72Hz	46MHz								
2	60Hz	63MHz	1024 × 768	0.25	0.5	1	2	2	3 **	4 **
	72Hz	76MHz								
4	60Hz	105MHz	1280 × 1024	0.5	1	2	3 **	3 **	4 ***	6 ***
	72Hz	126MHz								
4	60Hz	164MHz	1600 × 1280	0.5	1	2	4 **	4 **	6 ***	8 ***
	72Hz	197MHz								
NUMBER OF COLORS				4	16	256	32K	64K	16M	16M + 256 OVERLAY
NUMBER OF BITS PER PIXEL				2	4	8	15 (16)	16	24	32

* AT APPROX 45MHz VRAM SERIAL PORT SPEED
** NEEDS PALETTE WITH 64-BIT PIXEL PORT OR EXTERNAL MUX
*** NEEDS PALETTE WITH MORE THAN 64-BIT PIXEL PORT AT PRESENT VRAM SPEED OR EXTERNAL MUX

Figure 2.39 - Resolution, Colors and Frame Store Size

6.3 Video Interface Palettes Product Range

TI produces a substantial range of Video Interface Palettes with new devices constantly under development to keep pace with the rapidly developing PC market. Figure 2.40 shows some of the main features of these products.

Video Interface Palette Products

Device	Pixel Bus Width (bits)	Pixel Clock Max. (MHz)	Features
TLC34058	32	135	Industry standard, second source to BT458
TLC34074	32	200	Big & Little Endian format,8-bit DAC
TLC34075A	32	135	24-bit true color
TLC34076	32	170	"Enhanced" '34075, 16 & 24-bit true color
TLC34077	32	135	TLC34076 for ATI68800 controller
TVP3010	32	170	TLC340xx comp., H/W cursor, VRAM interface, direct & true color
TVP3020	64	200	H/W cursor, VRAM interface, direct & true color
TVP3025	64	220	TVP3020 + clock PLLs, BT485 register emulation for S3-Vision964
TVP3026	64	220	Cost optimised TVP3026, BT485 driver comp., packed pixel support
TVP3030	128	220	TVP3026 + dual PLLs, additional packed-pixel modes, 128-bit
TVP3409	16	170	Low cost for DRAM based systems, PLL synthesisers, comp. to ATT20C409
TVP3703	16	170	Low cost for DRAM based systems, PLL synthesisers, comp. to STG1703

Figure 2.40 - Video Interface Palettes Product Range

Section 3
Power Supply Solutions

Contributions by
Horst Schwahn
Ingrid Kohl
Tim Ardley

TEXAS INSTRUMENTS

Contents Section 3

1. TLE2425/6 - Virtual Ground Generators

1.1 Single Supply Operation

There are applications where operation from a single 5V supply is mandatory. If this is the case, careful consideration needs to be paid to the voltage at which the inputs of the op amp are biased.

Normal dual supply op amps in an inverting configuration will have their inputs biased around 0V, allowing the output to swing symmetrically around 0V.

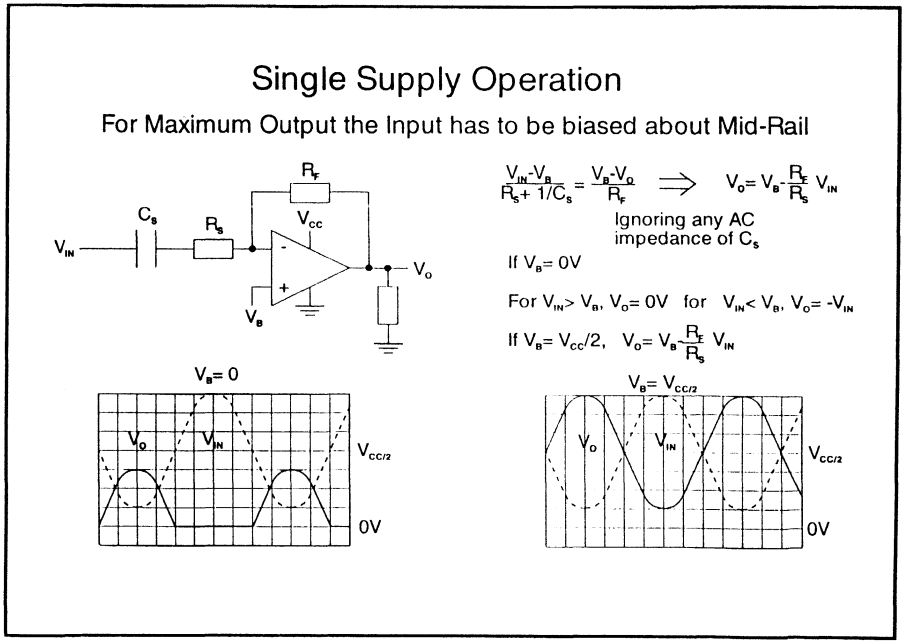


Figure 3.1 - Single Supply Operation

However, if an op amp operating from a single 5V supply has its inputs biased around 0V, then positive input voltages will drive its output into saturation just above 0V. Negative input voltages will drive the output into its normal positive output swing.

Therefore, operating from a single supply voltage, inputs must be biased at around half the supply voltage. Figure 3.1 shows the effects of biasing the inputs at 0V and at half the supply voltage. When biasing the single supply opamp with its input at half the supply voltage the loading of the feedback resistors must be taken into account. The feedback resistor will be treated as a load by the op amp; if the loading is too great crossover distortion could be introduced.

1.2 TLE2425/6 - Virtual Ground Generators

Single supply applications require an accurate reference, which will need to be able to supply varying amounts of current.

The TLE2425 contains an accurate low power 2.5V reference that is buffered by a low-power op amp capable of high output current. This makes it ideal for 5V supply applications where either a low power reference or a low impedance artificial ground is required. The TLE2425 requires only 170µA of quiescent current, but is capable of sourcing more than 20 mA of output current. Further, the TLE2425 has been designed to drive capacitors of up to several hundred microFarads.

The TLE2426 is very similar to the TLE2425 except that it contains a high impedance potential divider. This provides an 'Analogue Ground' equal to half the voltage applied across its IN and COMMON terminals.

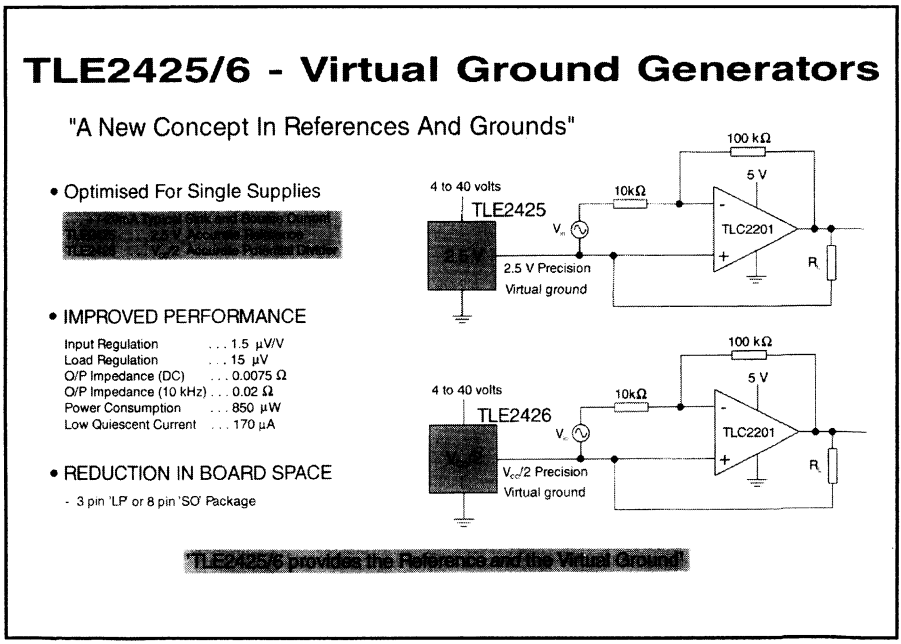


Figure 3.2 - TLE2425 & TLE2426 Features

Figure 3.2 shows the features of the two virtual gound generators, TLE2425 & TLE2426. We can readily see that these simple integrated circuit elements offer a novel function for signal conditioning circuits.

1.3 Unbalanced Power Supply Correction

All op amps are five terminal devices: the positive and the negative (ground) supply pins, the two inputs and the output. The op amp itself has no ground pin and therefore has no direct relation to the system ground, but only to half of the total supply voltage. Most op amps have been designed for their inputs to work in the middle of the supply voltage range, hence their datasheet parameters are tested and specified only at this mid-supply point. If op amps are operated with unbalanced supplies, the performance actually achieved in the application may be different from that specified in the data sheet. Typical errors seen will be increased common-mode errors, loss of symmetry in output swing or even clipping.

The TLE2426, by halving the total power supply, can be used as a half-supply analogue ground. Referring both the inputs and loads to this ground reduces the common-mode errors as well as the loss of symmetry in output swing.

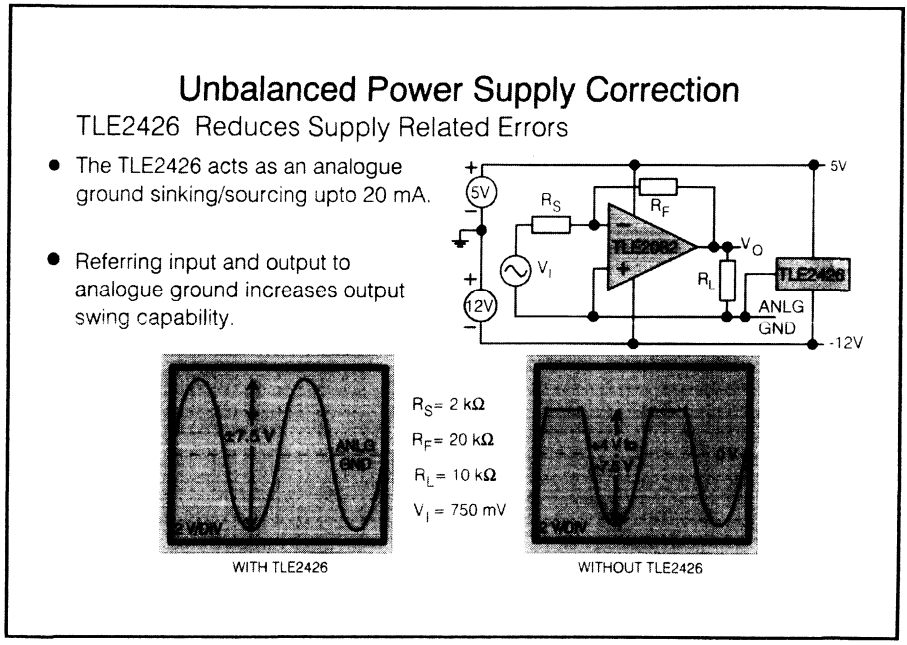


Figure 3.3 - Unbalanced Power Supply Correction

An unbalanced supply will have one supply greater than the other (+5V, -12V), as shown in figure 3.3.

An op amp, whose input is referred to ground, will have a much greater negative output swing than a positive one (i.e. the waveform is clipped). The use of TLE2426 in providing a true low impedance ground allows both the inputs and outputs of the op amp to be referred to the new ground and provide a symmetrical undistorted wave form. The TLE2082 is specified to drive a minimum of 30mA without problems in this application. The TLE2426 may be similarly used for other unbalanced supplies.

1.4 TLE2425 Current Source

The TLE2425 is ideal for maximising the performance of single rail 5V applications. Its accuracy and high output current make it well suited to function as a high performance current source. The minimum drop-out voltage of this device is 1.5V. The maximum output voltage of the TLE2425 is 13.5V. This means that the maximum voltage on the common terminal will be 11V. The feedback loop around the opamp means that the voltage at the inputs of the opamp will also be at 11V.

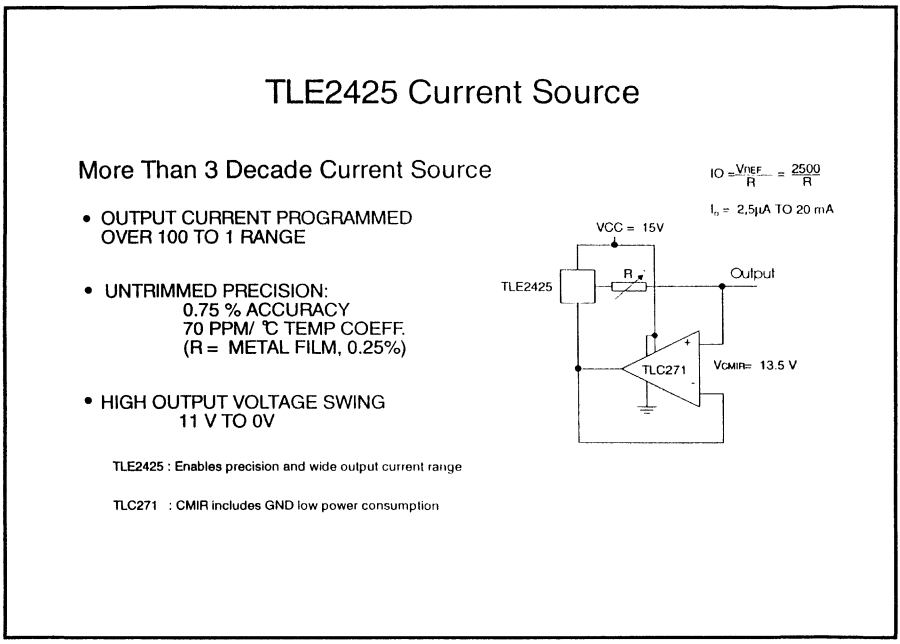


Figure 3.4 - TLE2425 Current Source

The common mode input voltage range (Vcmir) of the TLC271 extends from ground up to 1.5V from the positive supply. The positive supply is 15V therefore the specification of the TLC271 will be met for this parameter. To minimise the quiescent current of the whole current source, the TLC271 has its bias select pin (8) tied to the positive supply voltage.

The accuracy of the system is limited by the accuracy of the resistor, and by the input offset voltage of the TLC271 which will be also affected by its common mode rejection ratio.

2. Low Drop-Out (LDO) Regulators

2.1 Single supply powered applications

Many applications today are battery powered. The output voltage of the battery varies with the amount of current being removed from the cell. This effect based on the internal series resistance of the battery which changes with its remaining charge. In order to provide a 5V supply, 5 NiCd batteries have to be used. At initial full charge, the total battery voltage would be up to 7.5V. However, the nominal voltage for NiCd batteries in use is 1.2V which would equate to 6V. This is too high for 5V digital/linear electronics where the maximum supply is specified at 5.25V. Therefore, a fixed 5V output regulator must be used.

Major concerns of designers are: battery life and component dimensions.

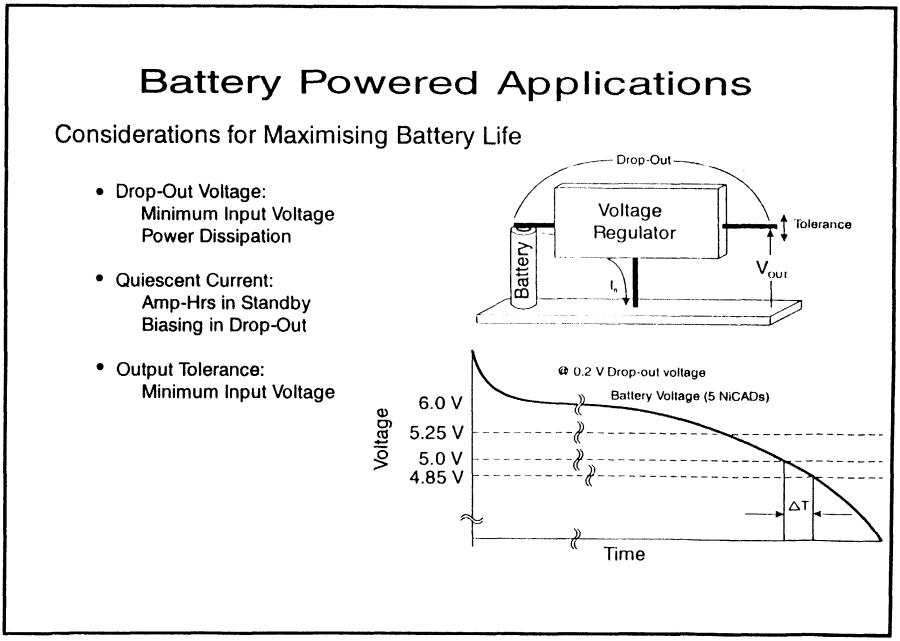


Figure 3.5 - Battery Powered Applications

2.2 Low drop-out voltage

Reducing the drop-out point of the linear voltage regulator extends the life of the battery by allowing the regulator to function longer from a lower input voltage. When the regulator enters its drop-out condition, the regulator's quiescent current will increase due to the reduced current gain of the pass transistor. Low drop-out regulators using PNP transistors have the base drive circuitry below the output voltage, thus allowing a much lower drop-out voltage.

2.3 Low power stand-by mode

To further extend the battery life of a portable system the device should have a TTL or CMOS compatible enable pin to switch the device into a standby operating mode. This facility can be used to automatically power down the system when it is not in use so that battery power is conserved.

2.4 Lower supply voltage

Using an output voltage of 4.85V instead of 5V for a regulator can add to the battery life of a system. This is due to the TTL tolerance being between 4.75 - 5.25V. If the supply is operated at 4.85V, the battery voltage can fall to a lower level while the regulator maintains a regulated output to the system.

2.5 TL75LPxx family (LDO)

The dropout voltage from the TL75LPxx family is lower than that from standard series regulators with NPN pass transistors. This permits regulation at lower battery voltages and thus increases the useful battery life. The key features of the TL75LPxx family are low dropout voltage and low power requirement in standby mode. Another feature is that all devices are available in 20-pin TSSOP package which allows high density layouts to be achieved on the PCB.

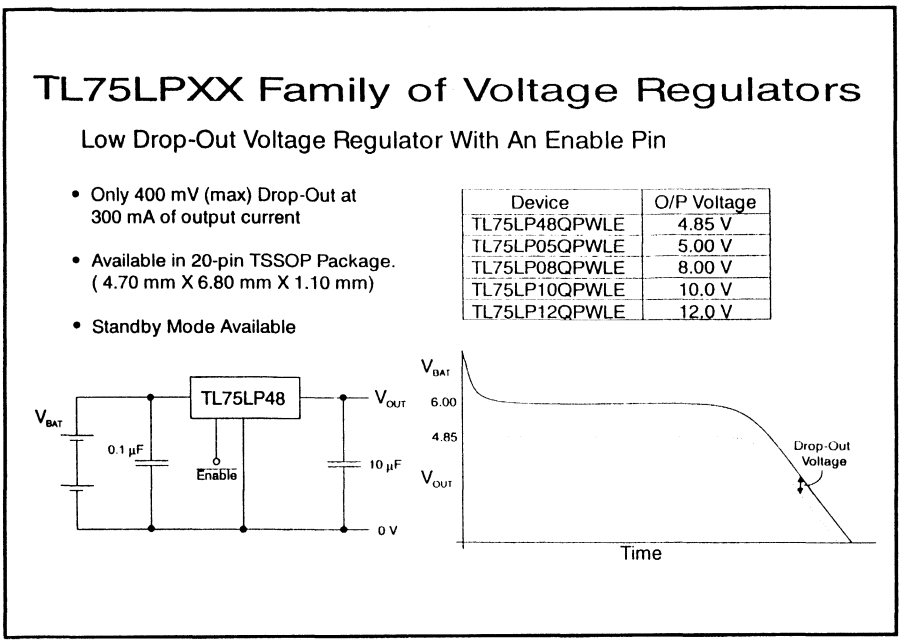


Figure 3.6 - TL75LPxx Low Dropout Regulators

The drop-out voltage for the TL75LPxx family is typically 220 mV @ 300mA of output source current. The product family also has an enable/disable pin which places the output part of the voltage regulator into a high impedance state. In this condition, the voltage regulator will only consume a typical current of 100 µA. The standby mode is TTL and CMOS compatible.

The TL75LP48 is specified at 4.85 V, and the 2% (max.) tolerance of the voltage regulator gives a minimum output voltage of 4.75 V which is the minimum supply voltage for TTL.

The input and output capacitance loading is important to the performance of this regulator type. The capacitance values and equivalent series resistance (ESR) affect the control loop of the device and therefore must be defined for the load and temperature range.

The TL75LPxx family only requires a minimum output load capacitance of 10 µF. This capacitor saves board space and costs less than the 100 µF capacitor formerly needed.

2.6 TLV2217-33 (LDO)

The 3.3 V supply voltage is currently preferred to 3 volts since this has full JEDEC standard approval. The TLV2217-33 is a low drop-out 3.3 V fixed output voltage regulator and meets the JEDEC standard. The device has a max. drop-out voltage of 500 mV while sourcing 500 mA of output current. Since the drop-out voltage is low, the minimum input voltage can be 3.8 V which makes it also suitable for running off existing 5V supplies.

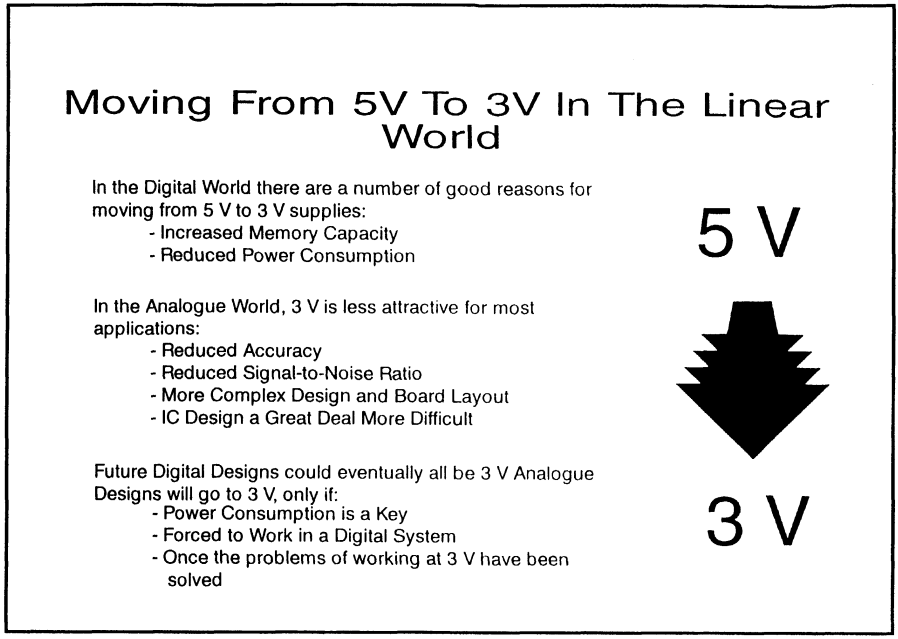


Figure 3.7 - 5 Volt to 3 Volt Transition

The output voltage tolerance is 1% at Tj = 25°C which guarantees an accurate output voltage. The TLV2217-33 requires input and output decoupling capacitors to make the voltage regulator stable. The minimum input capacitor value is 0.1 µF while the typical output value is 22 µF. The device is available in the TSSOP package for high density applications.

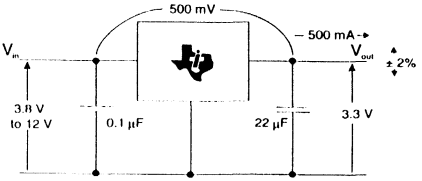
TLV2217-33 Voltage Regulator

3.3 V Low Drop-Out Fixed Output Voltage Regulator

- Meets the New 3.3 V JEDEC Standard.
- Available in the New TSSOP (surface mount package)
- 500-mV dropout at 500 mA

Application Areas

- 3.3 V from existing 5 V supplies.
- Medium power 3.3 V hand-held systems.
- 3.3 V High density applications



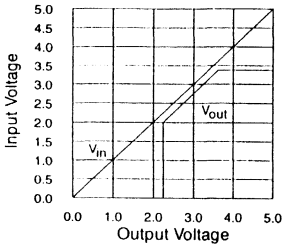


Figure 3.8 - The TLV2217-33 Voltage Regulator

The TLV2217-33 has a typical bias current of 2 mA with no load output current. In mains powered applications this parameter is not too critical. In battery powered applications however, the bias current under no load is regarded as a significant power loss and needs to be as low as possible. The device does not have an enable pin to place the device into a standby mode like the TL75LPXX. Another solution to reduce the power loss would be to insert an electronic switch (FET) between the power source and the input of the regulator. This will reduce the standby bias current of the TLV2217-33 to negligible levels.

To increase the output current capability (current boost) of the TLV2217-33, a shunt transistor can be used as shown in figure 3.8. The value of R is selected so that Q1 is off when the LDO is operating well within its maximum current output and power dissipation capability. Above the current capability of the LDO the current through R is sufficient to generate approx. 0.7 V (V_{BE}), and therefore the transistor Q1 starts to conduct, increasing the current capability to the load. The bias current of the transistor must go through the TLV2217-33. This needs to be considered when calculating R. It must also taken in account that adding of R at the input of the LDO regulator will increase the drop-out value from 0.5 Vmax. to about 1.2 V. This design idea has the benefit of keeping the output voltage of 3.3 V ±2% max. while offering higher levels of output current.

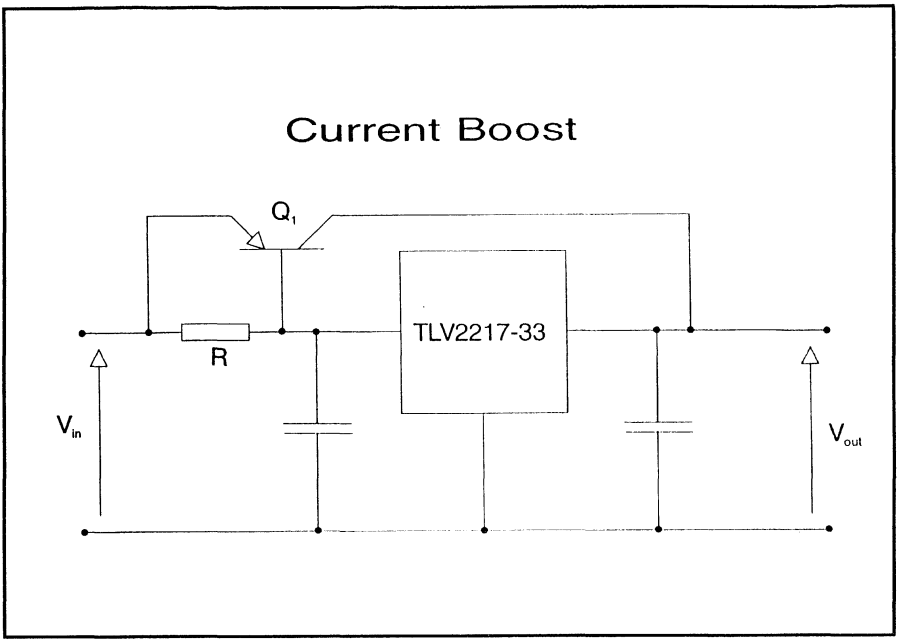


Figure 3.9 - TLV2217-33 Current Boost

2.7 TPS7101/33/48/50 (very low dropout)

The 3.3 V supply is dictated by the needs of the digital system. There are a number of reasons why moving to 3 V is attractive for the digital system. High component densities and speeds dictate smaller transistor geometries which can only sustain lower breadkdown voltages. Thus, the trend is to ever lower voltage components to realise these digital benefits.

2.7.1 Product Descripton

TheTPS71xx family of low drop-out (LDO) regulators offers an order of magnitude improvement in drop-out voltage over traditional bipolar designs. These devices feature a maximum dropout voltage as low as 32 mV at 100 mA of output current while maintaining a maximum quiescent current of 350 μA, regardless of load, even in drop-out. This exceptional performance is achieved by using a PMOS pass transistor instead of a bipolar PNP transistor. Using these LDOs directly adds operating life to equipment powered by fixed voltage battery supplies. An enable function allows for powering down the regulator and reduces sleep-state current to < 1 μA. There is also a power-good (PG) output that can be used as a power-on reset or as a low battery indicator.

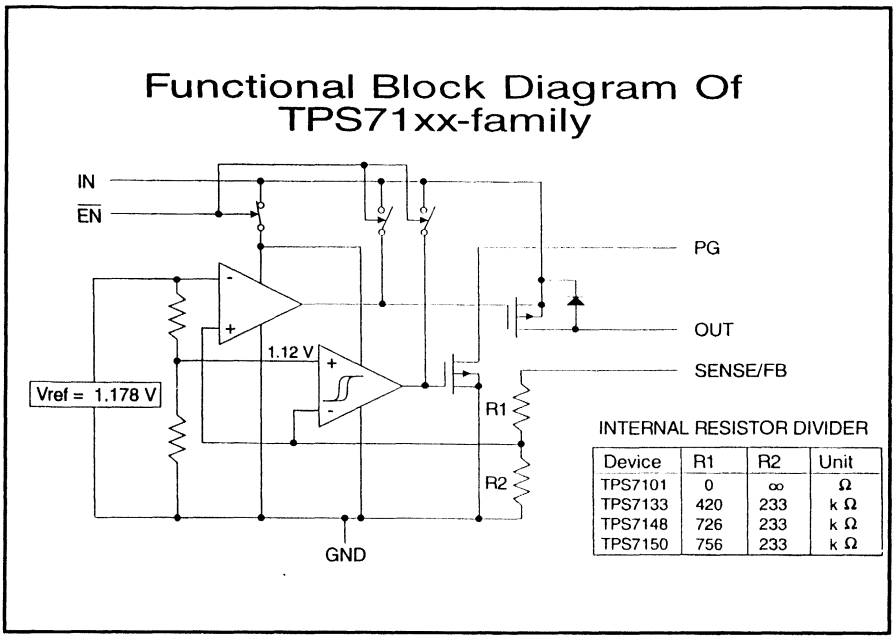


Figure 3.10 - TPS71xx Family Block Diagram

2.7.2 Key features / benefits

Using the Texas Instruments LinBiCMOS™ process technology the following device features are achieved:

- Industry's best available drop-out voltage on chip
- Extremly low and constant current, independent of load, even in drop-out
- 2% output regulation over full range of load, voltage and temperature
- Output current range of 0 mA to 500 mA
- Logic shutdown, sleep-state current < 1 µA
- Small 10 µF compensation capacitor at the output
- TSSOP packaging for space-critical designs

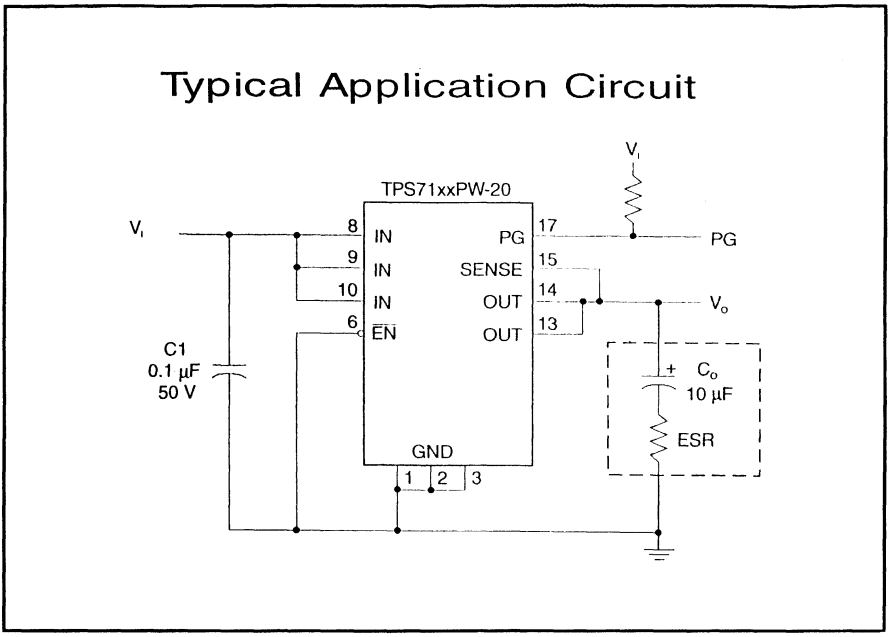


Figure 3.11 - TPS71xx Typical Application

2.7.3 Application information

The TPS71xx series contains three fixed and one adjustable version:

TPS7101	adjustable from1.2 V to 9.75 V
TPS7133	3.3 V
TPS7148	4.85 V
TPS7150	5.0 V

The main applications for this device family are notebook PCs, cellular phones, portable instruments and diagnostic and monitoring equipment.

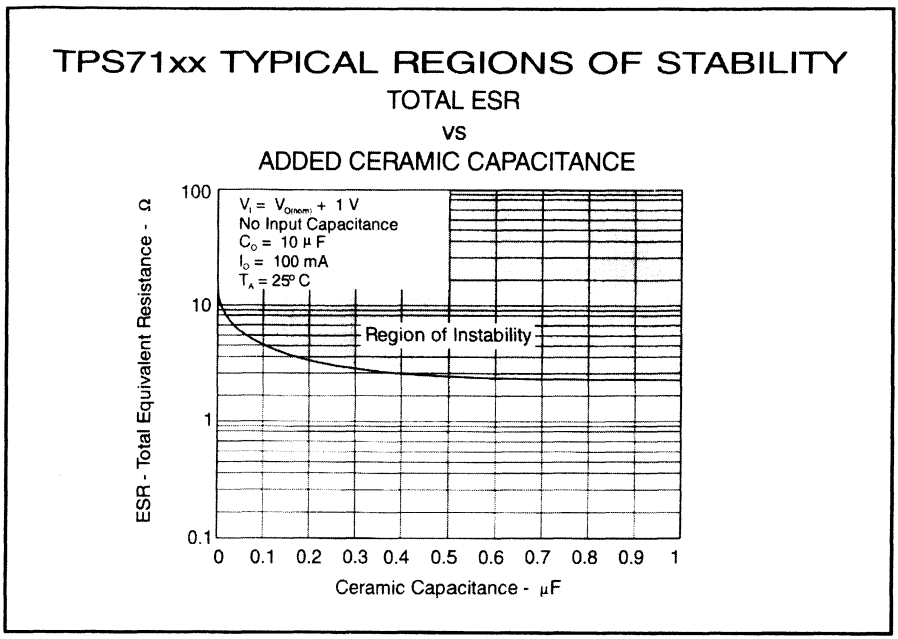


Figure 3.12 - TPS71xx Typical Regions of Stability

2.7.3.1 SENSE pin

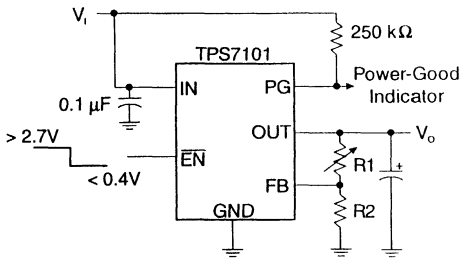
The SENSE pin of fixed-output LDO must be connected to the regulator output for proper operation of the regulator. The connection should be as short as possible. Internally, the SENSE pin connects to a high impedance wide-band amplifier through a resistor divider network. Routing the SENSE connection to minimize noise pickup is essential. An R-C network between SENSE and OUTPUT is not recommended as this may cause oscillation.

2.7.3.2 External capacitors

Normally, an input capacitor is not required. To improve load transient response and noise rejection a ceramic capacitor (0.1 μF) could be useful as a large load and fast rise time are anticipated.

As with most LDO regulators, the TPS71xx requires an output capacitor for stability. A low-ESR 10 μF solid-tantalum capacitor, connected from the regulator output to ground, is sufficient to ensure stability over the temperature range. Adding high frequency ceramic or film capacitors (such as power supply bypass capacitors for digital and linear ICs) can cause the regulator to become unstable unless the ESR (Equivalent Series Resistance) of the tantalum capacitor is less than 1.2 Ohm over temperature. Capacitors with published ESR specifications are available on the market for instance from Sprague, Kemet, AVX. Figure 3.12 shows typical regions of stability for the TPS71xx series.

TPS7101 Adjustable LDO Regulator Programming



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	Unit
2.5 V	191	169	k Ω
3.3 V	309	169	k Ω
3.6 V	348	169	k Ω
4 V	402	169	k Ω
5 V	549	169	k Ω
6.4 V	750	169	k Ω

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \cdot R2$$

Figure 3.13 - Programming the TPS7101 Adjustable LDO

2.7.3.3 TPS7101 Adjustable LDO

Programming the adjustable regulator is accomplished using an external resistor divider as shown in figure 3.13. The equation below defines the output voltage:

$$Vo = Vref\left(1 + \frac{R1}{R2}\right)$$

where V_{ref} = 1.178 V typ. (reference voltage).

Resistors R1 and R2 should be chosen for approximately 7 µA divider current. Recommended values for the resistors R1 and R2 are shown in figure 3.13.

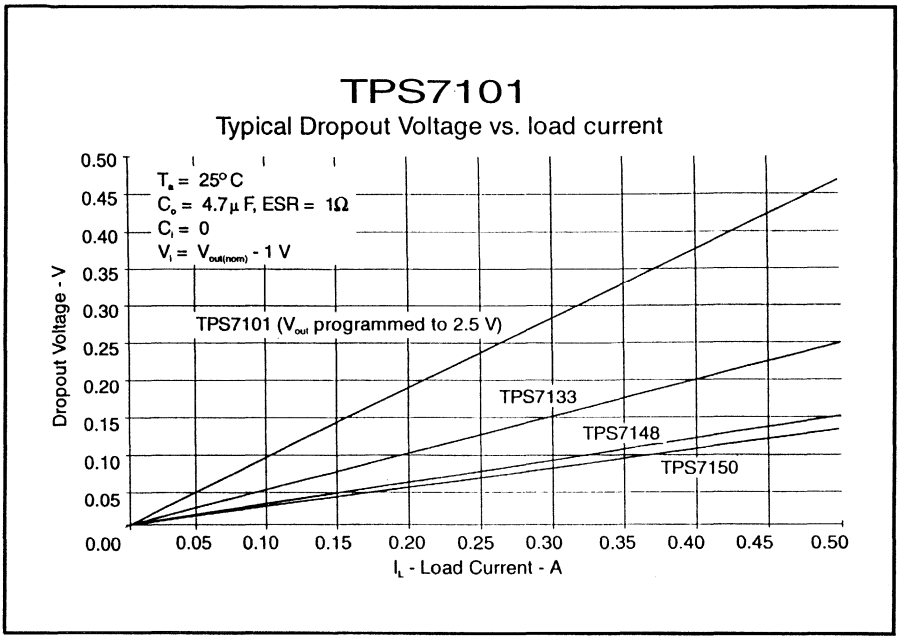


Figure 3.14 - TPS7101 Dropout Voltage vs. Load Current

2.7.3.4 Power good indicator

The status of the regulator output voltage can be monitored at the power-good (PG) output pin. The internal comparator comprehends the output voltage. When the output drops to between 92% and 98% of its nominal regulator value, the PG output transistor turns on, taking the signal low. The open-drain requires a pullup resistor (ca. 250 kOhm). If not used it can be left floating. Also PG can be used to drive power-on reset circuitry or as a low-battery indicator.

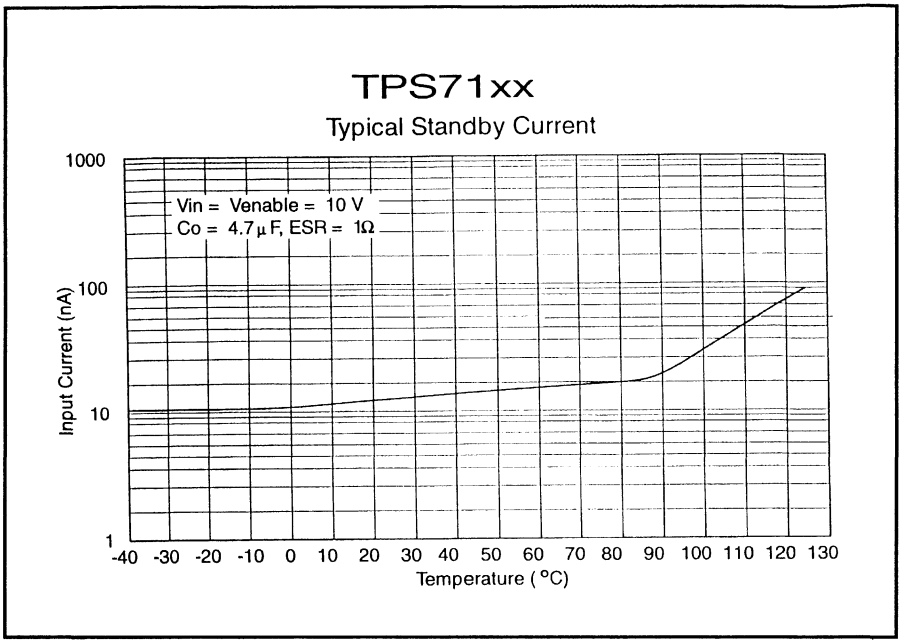


Figure 3.15 - TPS71xx Standby Currents

2.7.3.5 Regulator protection

The TPS71xx PMOS pass transistor has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (e.g. during power-down). If extended reverse voltage is anticipated, external limiting may be appropriate.

These devices also feature internal current limiting and thermal protection if the temperature exceeds 165°C. During normal operation, the TPS71xx limits output current to approx. 1 A.

When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Care should be taken not to exceed the power dissipation ratings of the package.

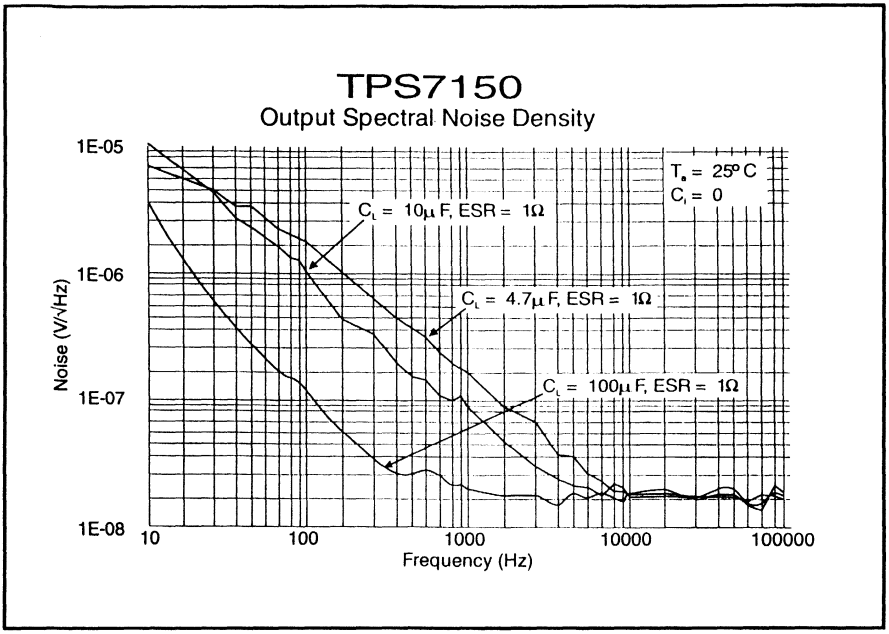


Figure 3.16 - TPS7150 Output Noise Spectrum

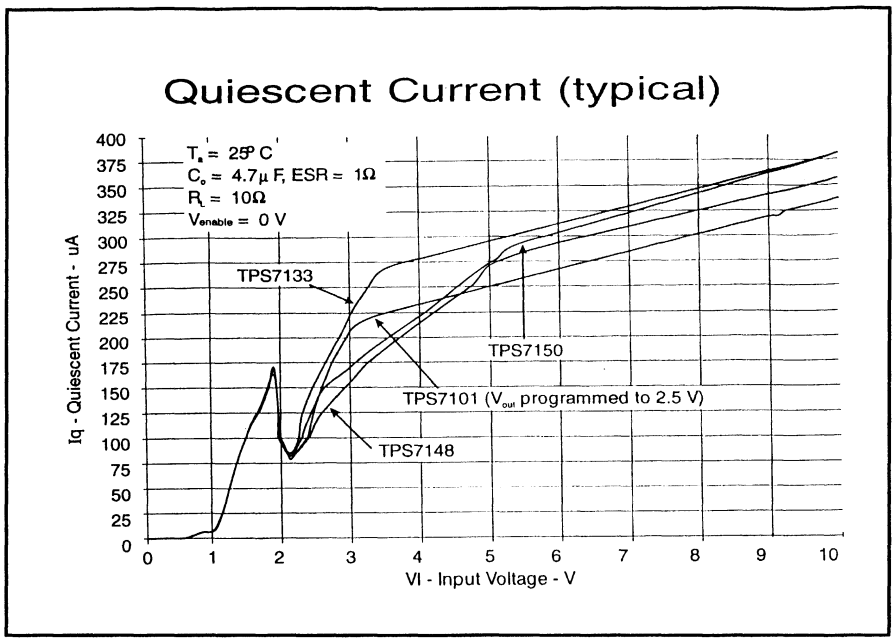


Figure 3.17 - TPS71xx Quiescent Current

2.8 TPS72xx series (very low dropout)

The TPS72xx family of LDO voltage regulators offers the benefits of low drop-out voltage, micro-power operation and miniaturized packaging. Packaged in 8-pin TSSOP and SOIC, the TPS72xx series of very low drop-out regulators are ideal for cost sensitive designs (compared to the TPS71xx family) and where board space is at a premium.

2.8.1 Product description

The PMOS pass element behaves as a low value resistor, the drop-out voltage is very low (90 mV) at 100 mA for the TPS7250) and is directly proportional to the load current. Therefore, the PMOS pass element is a voltage driven structure. The quiescent current is also very low (200 µA typically) and stable over the entire range of output load current. The quiescent current does not increase when the regulator goes into drop-out unlike PNP structured LDO regulators. This results in a significant increase in system battery operating life.

2.8.2 Application information

All the applications mentioned earlier for the TPS71xx family can be satisfied with the TPS72xx series if the recommended output current limit of 250 mA is taken into account.

The TPS72xx series also offer an extremely low sleep state current of 1 µA, and an error flag when the output voltage falls 5% below the nominal value. These features make

power supply design much easier and reduce development cost. Figure 3.18 shows a typical application schematic.

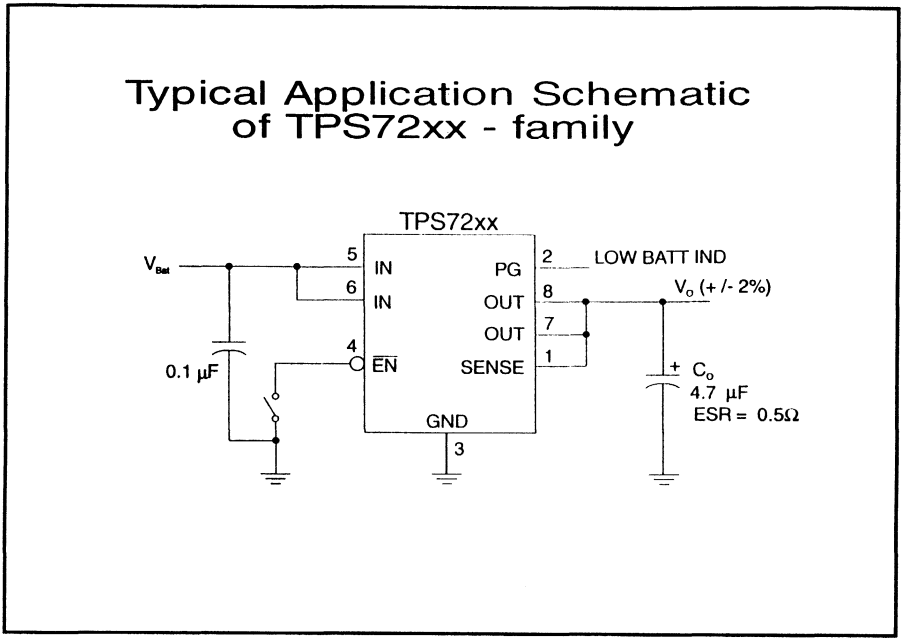
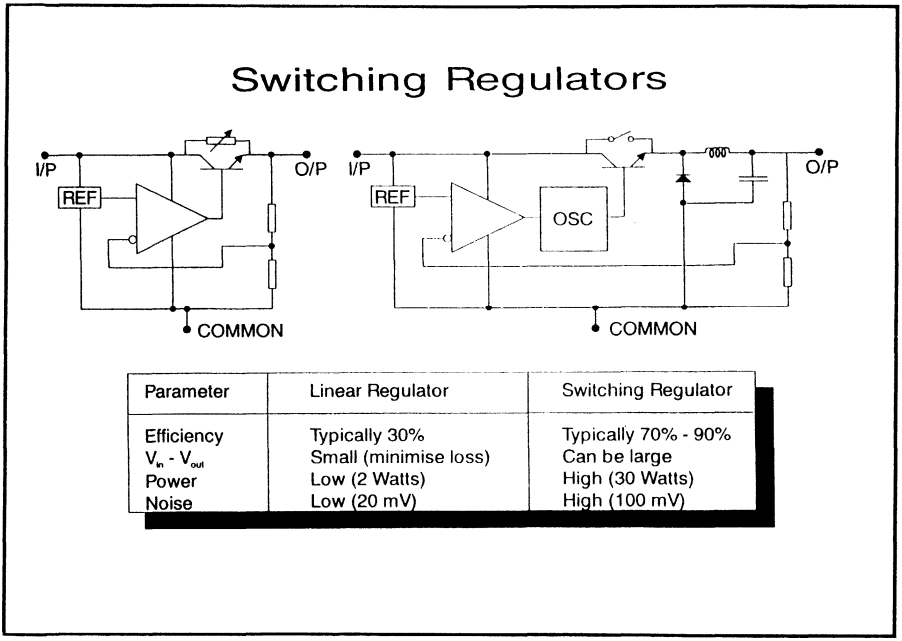


Figure 3.18 - TPS72xx Typical Application

3. Switching regulators (PWM)

3.1 Introduction

In a switching regulator a transistor acts as the control element. The control is provided by chopping the input voltage to control the energy ($\frac{1}{2}LI^2$) which is stored in the inductor, see figure 3.19.



Parameter	Linear Regulator	Switching Regulator
Efficiency	Typically 30%	Typically 70% - 90%
V_{in} - V_{out}	Small (minimise loss)	Can be large
Power	Low (2 Watts)	High (30 Watts)
Noise	Low (20 mV)	High (100 mV)

Figure 3.19 - Switching Voltage Regulators

The advantage of this technique is that the pass transistor is either fully switched off or on. In both cases the power dissipated in the switch is minimised. Therefore the PWM regulator operates at a higher efficiency than a series regulator. Typically, a switching regulator operates at 70% to 90% efficiency, compared to the 30% efficiency of a series regulator.

The disadvantage of a PWM regulator is that it is more complex and requires more complicated support circuitry. An inductor is used as the passive component to store charge instead of a capacitor, and inductor design is complex. The switching process also

introduces high frequency electrical noise on the input and output voltages, and filters are often needed. Finally, PWM regulators tend to produce more ripple at the output.

3.2 Switching PWM topology

There are four main types of configuration which generate a PWM output voltage.

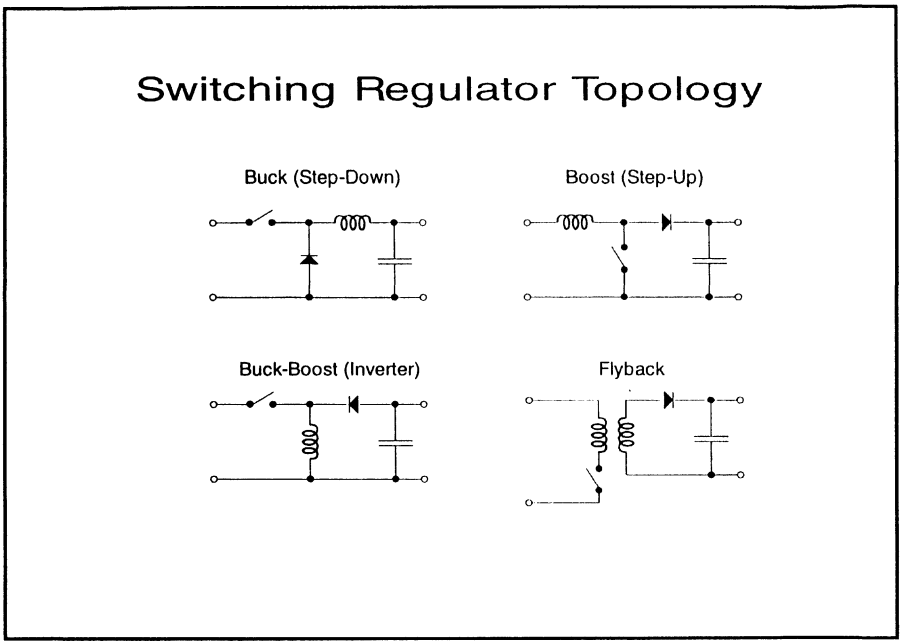


Figure 3.20 - Switching Regulator Topology

The Buck (Step-down) converter interrupts the current through the inductor to the load and therefore interrupts the voltage to the load. This means that the inductor voltage is either Vin or 0 V. A simple equation can be used:

$$Vout = Vin\left(\frac{Ton}{Toff + Ton}\right)$$

The Boost (Step-up) converter operates by storing energy in the inductor when the switch is closed, and transferring this stored energy to the load capacitor when the switch is open. This configuration allows the output voltage to be set to a greater voltage than the input voltage. Also for calculation purposes a simple equation can be used:

$$Vout = Vin\left(1 + \frac{Ton}{Toff}\right)$$

The Buck-Boost converter (Inverter) operates in almost the same way as the boost converter. Energy is stored in the inductor when the switch is closed. However, when the

switch is turned off, the energy is transferred through the diode to the load capacitor with a negative amplitude.

The Flyback converter uses the same principle as the boost converter. However, the inductor is now the primary winding of a transformer and the secondary winding is used as the output. Now the output voltage can be set by the winding relationship (1:N) between primary and secondary of the transformer.

3.3 Voltage mode PWM control

The control technique of the PWM regulator is provided by a feedback loop from an external potential divider network which is compared to an accurate internal voltage reference. The difference between the actual and the desired output voltage is then generated by a differential amplifier which produces an error signal (Verr). This error signal is compared to the oscillator voltage (Vosc) which resulted in a switched output voltage (Vpwm).

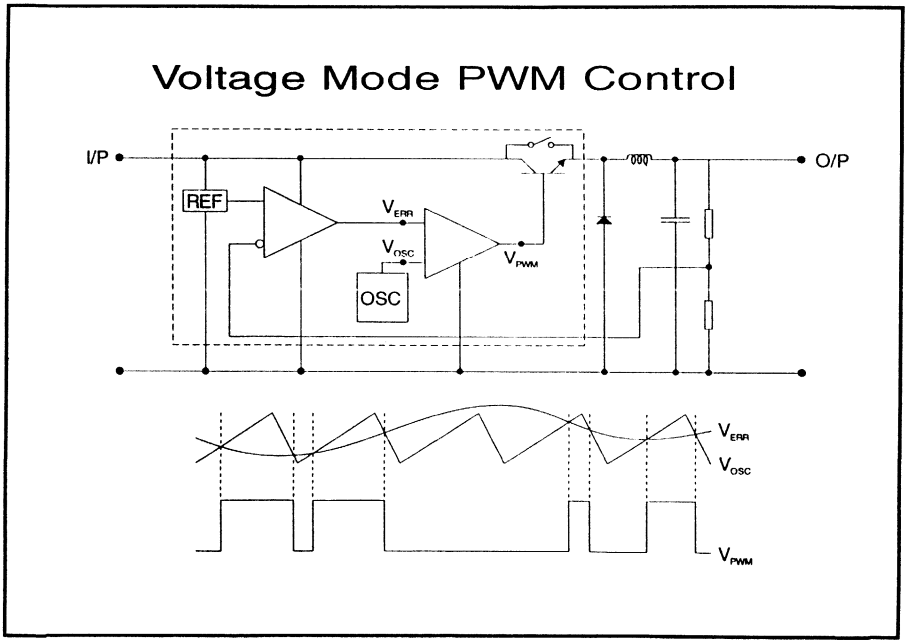


Figure 3.21 - Voltage Mode PWM Control

The frequency of the oscillator is normally controlled by an external timing capacitor. Whenever the magnitude of the voltage ramp exceeds that of the error signal, the comparator signal is high, activating the power switch. Similarly, when the ramp is below the error signal, the output is low and the switch is turned off. The width of the pulses (and hence the duty cycle) is modulated by the error signal. Owing to the increased need for switching regulators in portable and high density applications, Texas Instruments has developed a range of Voltage Mode PWMs.

3.4 TL5001 (PWM controller)

The TL5001 is a pulse-width modulation control integrated circuit. The high switching frequency (up to 400 kHz) achieves high efficiency with smaller, lower cost external components. Frequency and dead-time control use just one external resistor each. A low supply current of only 1.4 mA makes the device well-suited for DC-to-DC converters in battery-powered equipment.

Other features include:

- Wide input voltage range (3.6 V to 40 V) – supports 3 V design
- Short-circuit and undervoltage protection – improves system reliability
- Output current 20 mA – directly drives PMOS transistors
- High output voltage up to 50 V – supports range of circuits
- 8-pin surface-mount and DIP packaging – saves board space

This control circuit is primarily developed for Notebook PCs including LCD backlight supplies.

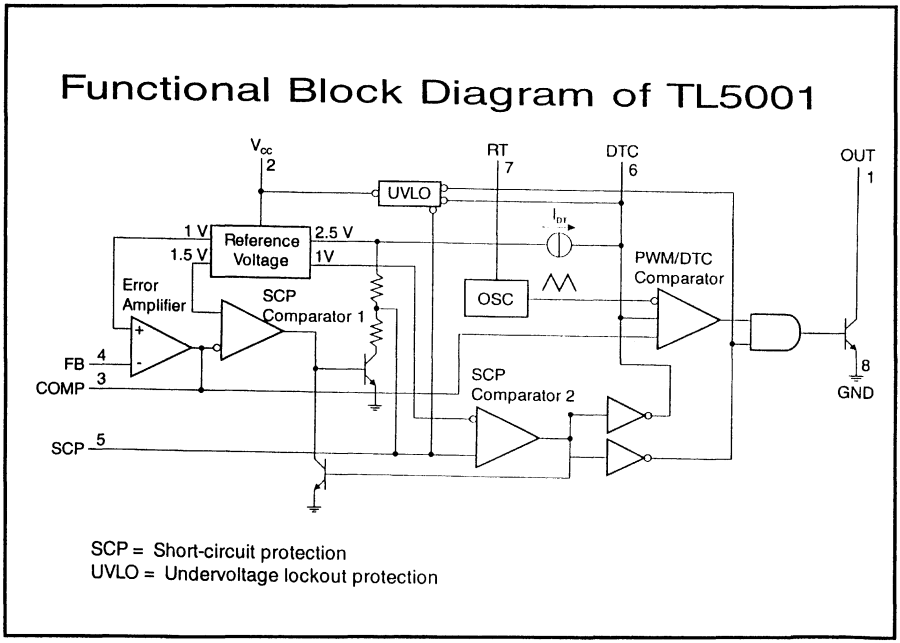


Figure 3.22 - TL5001 Block Diagram

3.4.1 Product description

The TL5001 incorporates all of the functions required to design a control circuit. The device can easily be used in step-up, step-down and flyback configurations to generate positive voltages.

Under-voltage lockout checks the outputs during the low V_{CC} conditions. Dead-time control is ajustable from 0% to 100% by connecting one external resistor between the DTC and GND pins.

A full description of use of the TL5001 in a 5-V to 3.3-V step-down converter, operating up to 0.75 A can be found in the application reort Library Reference SLVA034.

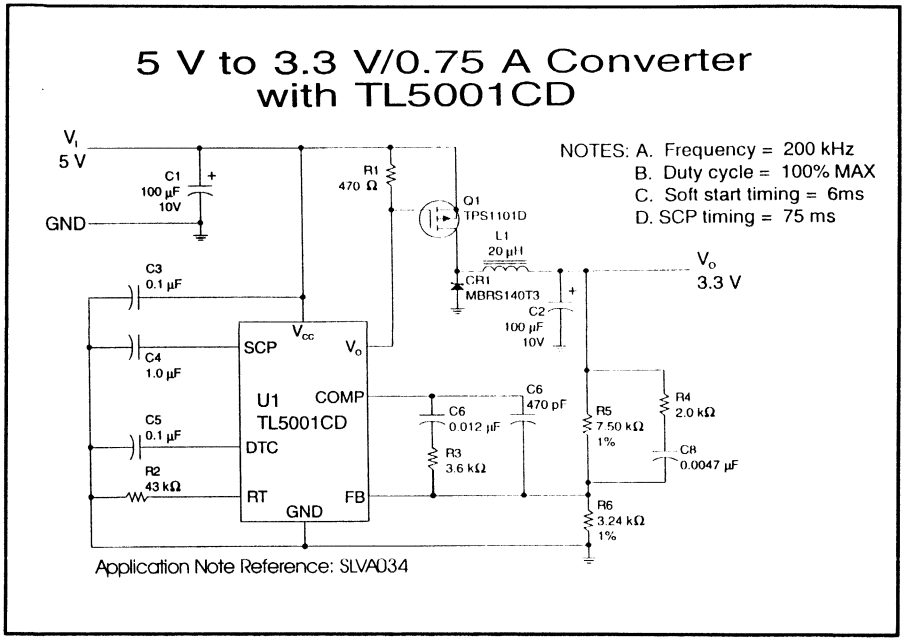


Figure 3.23 - 5-V to 3.3-V Step-down Converter

Test Results of DC/DC - Converter with TL5001

PARAMETER	TEST CONDITIONS	MEASUREMENT
Load regulation	V_I = 5 V, IO = 0 - 750 mA	1.4%
Output ripple (peak-to-peak)	IO = 750 mA	< 20 mV
Efficiency	V_I = 5 V, IO = 750 mA, Q1 = SI9405	74.4%
	V_I = 5 V, IO = 750 mA, Q1 = TPS1101	84.1% *

*The higher efficiency achieved with the TPS1101 is due to lower gate capacitance, which speeds up switching and reduces switching loss.

Figure 3.24 - Test results of TL5001 DC-to-DC Converter

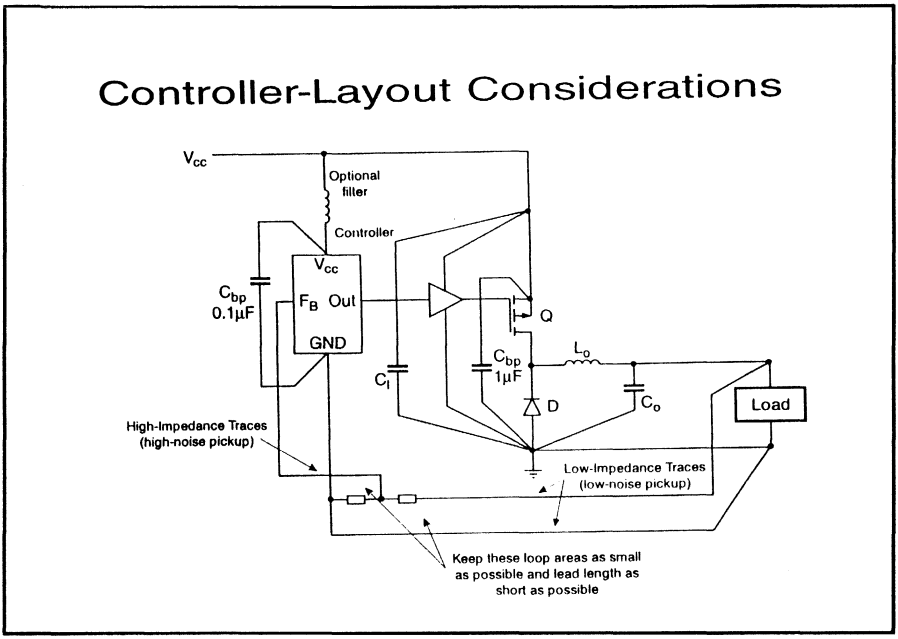


Figure 3.25 - TL5001 Controller Layout Considerations

3.5 TL1451AC dual PWM controller

Many of the systems require regulation of multiple supply rails with a minimum power loss in the regulator. The TL1451AC is especially suited for applications like office equipment, motor controllers, audio amplifiers, VCRs, microprocessor systems, etc.

3.5.1 Product description

The TL1451AC has on a single monolithic chip all the functions required to construct two independent PWM control circuits.

The TL1451AC is characterized over an operating temperature range from -20 to 85°C and contains: an adjustable oscillator, temperature-stabilized voltage reference, under-voltage lockout circuit, short-circuit protection comparator, dual error amplifiers, dual dead-time control circuits, dual PWM comparators and dual open-collector output transistors, each with 20 mA output sink capability.

Figure 3.26 shows the functional block diagram for the 16-pin package device.

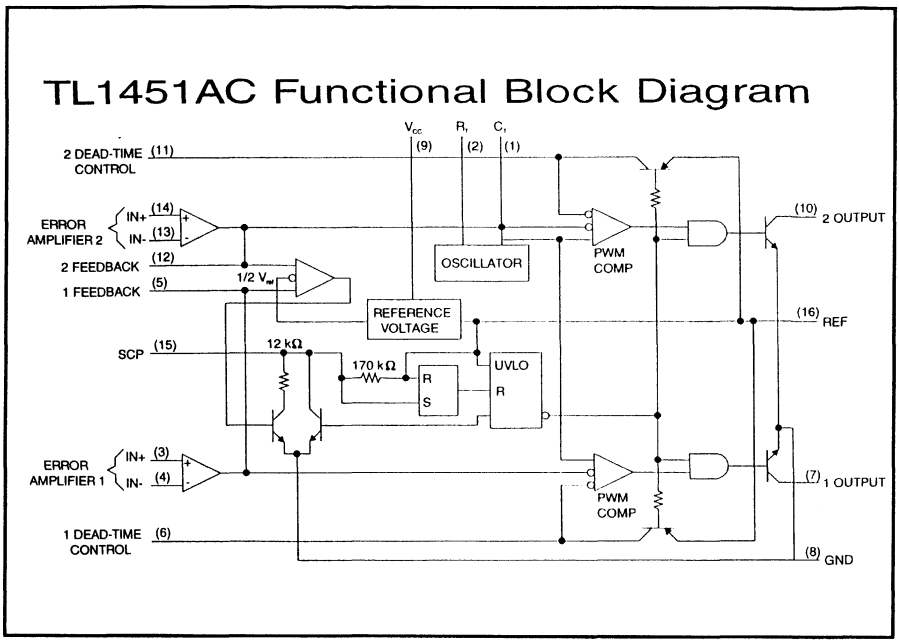


Figure 3.26 - TL1451 Block Diagram

Synchronizing the oscillator: Synchronising two or more oscillators in a common system is easily accomplished with the architecture of the TL1451AC. Since the internal oscillator is used for no other purpose than providing a symmetrically uniform triangular waveform on the timing capacitor, the internal oscillator can be disabled and a compatible triangular waveform can be provided at the timing capacitor terminal.

The internal oscillator can be inhibited by connecting the RT pin to the reference supply output pin.

Master-Slave synchronization: To create master-slave synchronization for two or more TL1451AC devices, establish one device as the master and program its oscillator in the normal manner. Disable the oscillators of each slave circuit and connect the master and slave timing capacitor pins together.

Reference regulator: The internal 2.5 V reference regulator is designed primarily to provide the internal circuitry with a stable supply voltage. It will also supply up to 10 mA supply current to an additional external load. The external load should not be excessive to avoid degrading the device performance. Reference voltage levels for the error amplifier and dead-time control inputs should be derived from the reference output.

Error-amplifier bias configuration: The TL1451AC is designed to employ both amplifiers in a non-inverting configuration.

TL1451AC Dual PWM Controller

- Dual Independent PWM controllers.
- Oscillator Frequency up to 500 kHz.
- Deadtime Control from 0% - 100%.
- Undervoltage Lockout of 3.6 V.

Application Areas

DC - DC Converters.

(Step-up Step-down, Inverter)

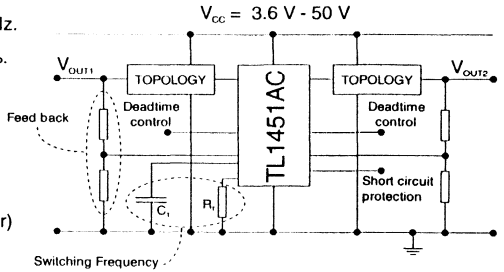


Figure 3.27 - TL1451 Configuration

Latched Short-Circuit Protection (SCP) with timer: The SCP circuit includes timer, latch and short circuit protection. The outputs of both error amplifiers are connected to the SCP comparator inputs as well as to the feedback pins 5 and 12. The error amplifier outputs are compared with the internally generated reference of approximately 1.25 V (V_{ref} / 2). Under normal operating conditions the error amplifier outputs are well above the 1.25 V protection comparator reference. If one or both of the error amplifier outputs goes low (below 1.25 V), indicating a short-circuit or heavy loading, the output of the protection comparator goes low. This turns off a transistor, allowing the external capacitor at the SCP-pin to charge-up toward V_{ref}. When the capacitor is charged to 0.6 V, the protection latch is set and the undervoltage lockout (UVLO) circuit is enabled. The UVLO output turns off the output drivers and sets the dead time to 100%. Figure 3.27 highlights important functional circuit blocks.

Soft start: Soft start reduces stress on the output switching transistors. This is caused by the start-up surge which occurs as the output filter capacitor charges. Soft start limits the energy available at the instant of turn-on and gradually allows it to increase. The available dead-time control facilitates soft start. Two external capacitors (one for each controller) perform the soft start function. They are connected between V_{ref} (pin 16) and the respective dead-time inputs (pins 6 and 11). For the capacitor value calculation please see the application report (SLVAE02).

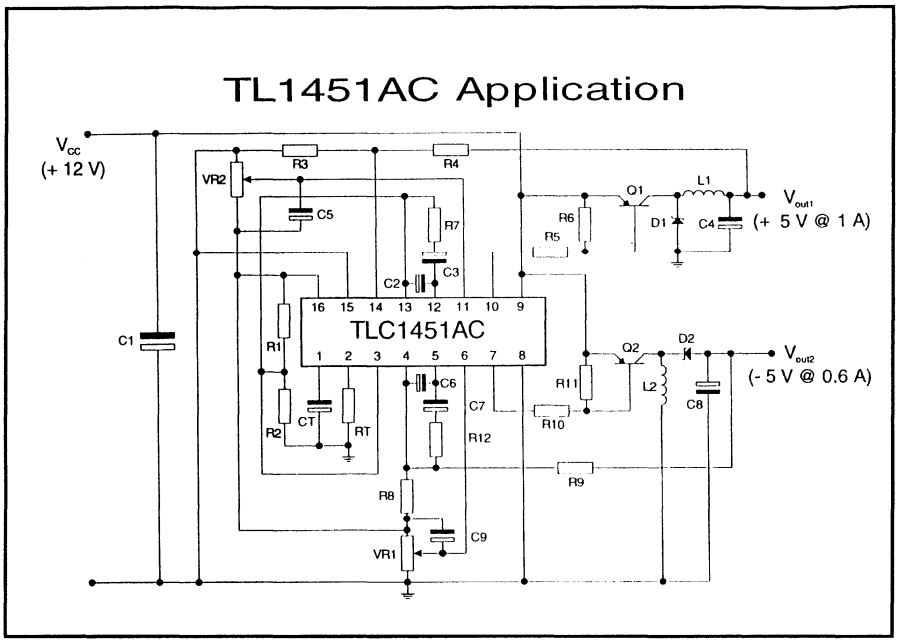


Figure 3.28 - TL1451AC Application

Further applications for dual flyback converters are in the application report:

One example converts 5V Vcc to 12 V output (at 0.7 A) with 80% minimum efficiency and to -5 V output (at 0.4 A) with 75 % minimum efficiency.

Another example shows the use of the TL1451 as a high-speed switching regulator converting a 12-V Vcc to 24-V and 5-V outputs.

3.6 TL1454AC dual PWM controller

3.6.1 Product description

The TL1454C incorporates on a single monolithic chip all the functions required in the construction of two PWM control circuits. The device contains a 1.25 V reference, two error amplifiers, an adjustable triangle-wave oscillator, two dead-time comparators, undervoltage lockout, short-circuit protection and dual totem-pole output circuits. See figure 3.29.

The output circuits can drive external power MOSFETs directly, output 1 for N-channel MOSFETs and output 2 for P-channel MOSFETs. The output stages are totem-pole outputs with a maximum source and sink current rating of 40 mA and a voltage range of 20 V. The output is controlled by a complementary output AND gate and is turned on (sourcing current for output 1, sinking current for output 2) when all following conditions are met: the oscillator triangle wave is higher than both the DTC voltage and the error amplifier output voltage, the undervoltage lockout is inactive and the SCP circuit is inactive.

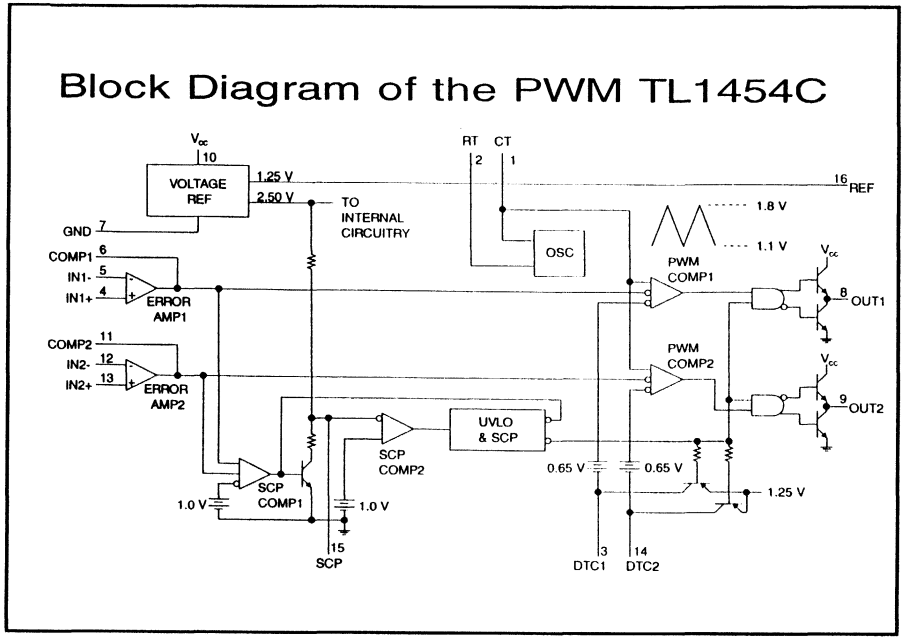


Figure 3.29 - TL1454 Block Diagram

3.6.2 Key features

- Oscillation frequency – 50 kHz to 2 MHz
- Wide supply voltage range – 3.6 V to 20 V
- Low supply current – 3.5 mA typ.
- 16-pin dual-in-line or SO package

3.6.3 Applications

The TL1454C can be used for the same applications as TL1451AC and also for additional applications where external MOSFET drivers are required. Another advantage may be the high oscillation frequency which shows the improved efficiency of the regulator. But care has to be taken regarding radiation effects on other parts of the circuit (short circuit connections!).

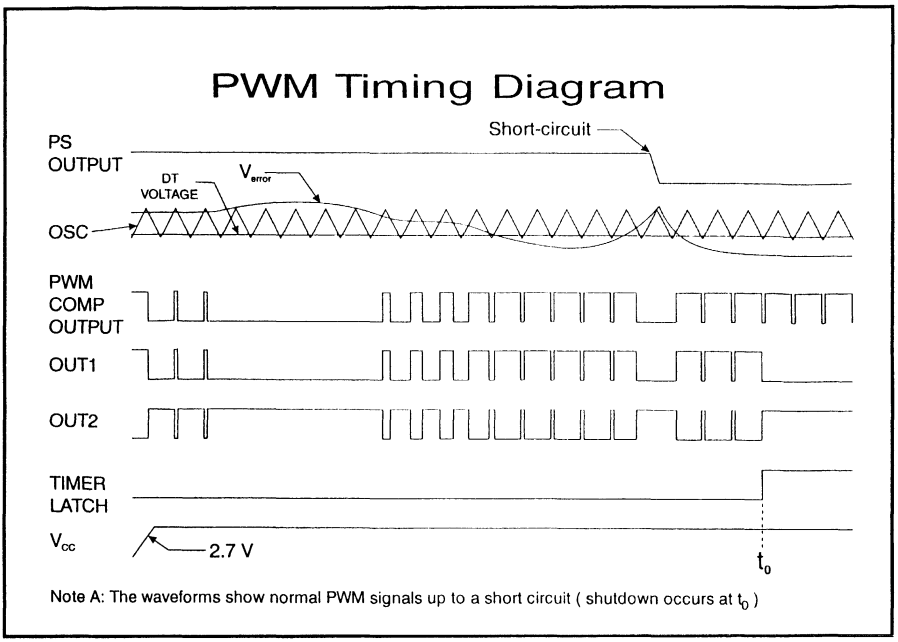


Figure 3.30 - PWM Timing Diagram

Figure 3.30 shows the waveforms of the normal PWM signals up to a short circuit (shut down occurs at t_0).

4. Supply Voltage Supervisors (SVS) SCSI-terminators, Clamp Circuits

4.1 Introduction

The function of a Supply Voltage Supervisor (SVS) is to monitor the supply voltage to a system and to flag the microprocessor, through its enable/disable facility, if the supply voltage goes out of its defined operating window. The supply voltage supervisor can also be used to ensure that a digital system is powered up correctly by applying a reset to the system until the supply has been established.

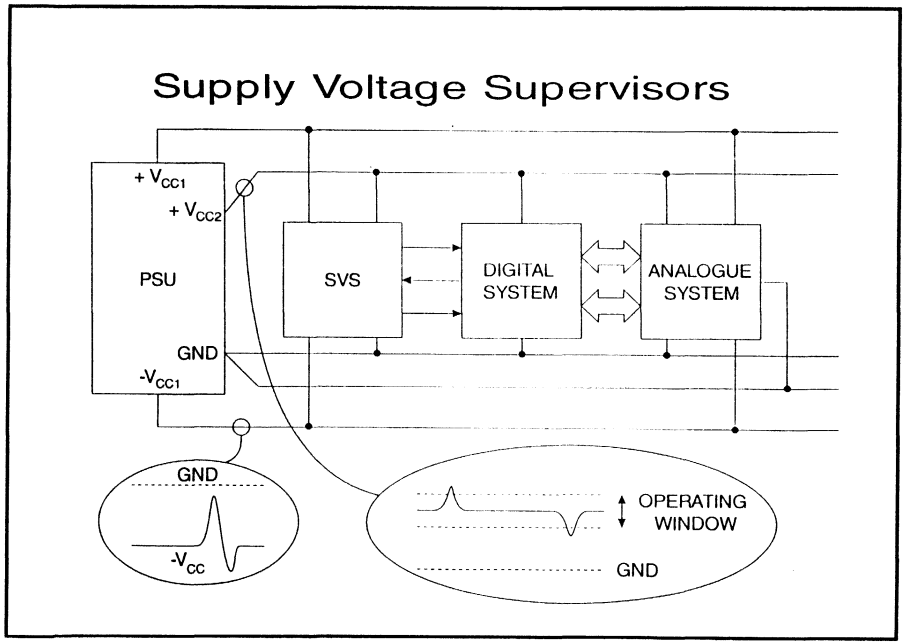


Figure 3.31 - Supply Voltage Supervisors

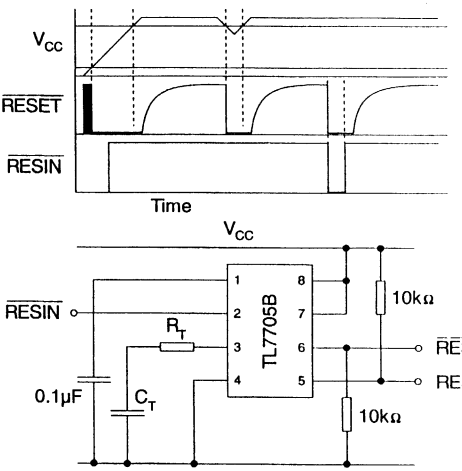
In an analogue system, variations in the supply can affect the performance of the signal to noise ratio and the dynamic range of the system. However, in a digital system where the supply voltage window is fixed at 5 V ±5% to guarantee its operation, any power

supply variation (under- or over-voltage) outside the specified window may cause unpredictable failures.

A power supply fault can affect any of the digital bits from the MSB to the LSB. Undervoltage is the most common condition, occurring each time the power supply is turned on. The output voltage takes time to settle to its required value and therefore the digital system would be powered up before the supply has settled within the specified window.

When the supply voltage of a linear regulator falls below the drop-out point, the output of the regulator generally tracks the input voltage, causing a negative spike to occur on the ouput (undervoltage fault).

Supply Voltage Supervisors



Device	Supply	Tolerance
TL7702A TL7705A TL7709A TL7712A TL7715A	Prog. 5V 9V 12V 15V	1%
TL7702B TL7705B	Prog. 5V	
TL7757 TL7759	5V 5V	2.6%
TL7770-5 TL7770-12 TL7770-15	5V + Prog. 12V + Prog. 15V + Prog.	1%
TLC7705I	5V	1.5%

Figure 3.32 - SVS Family

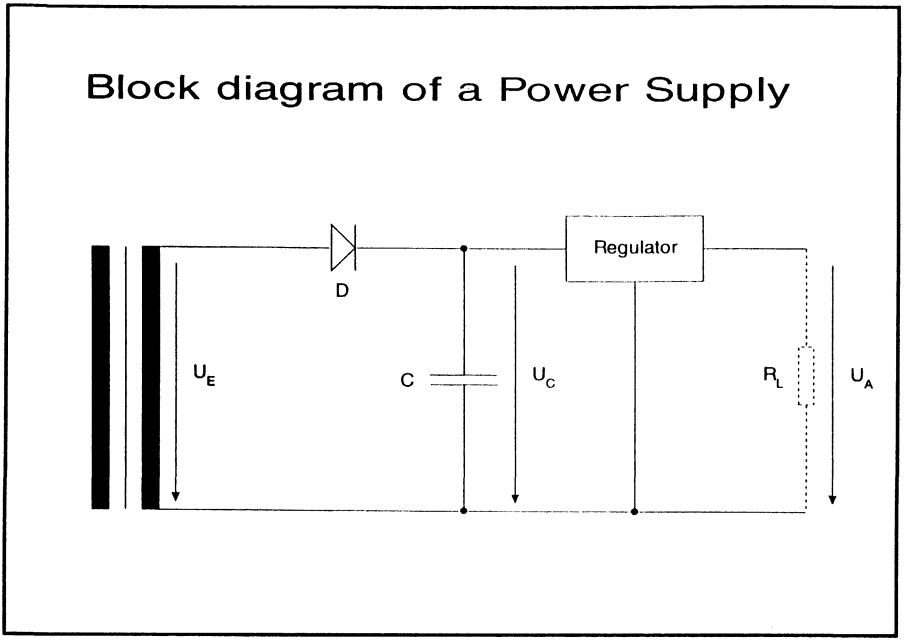


Figure 3.33 - Power Supply Block Diagram

4.2 TLC7705I low power SVS

For applications where low power dissipation is a need, TI has developed the TLC7705I. This is a BiCMOS version of a supply voltage supervision circuit and requires only a very low supply current.

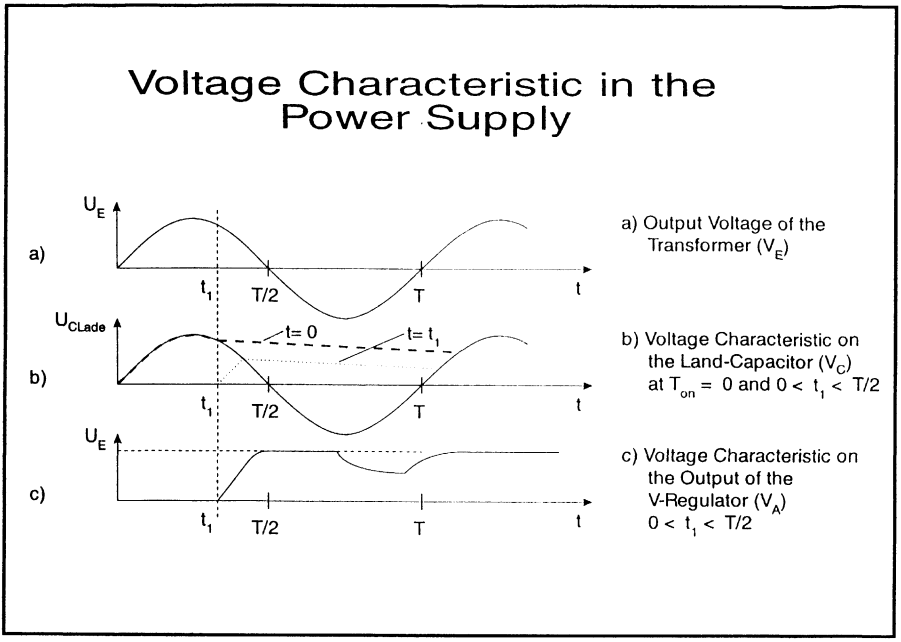


Figure 3.34 - AC / DC Supply Voltage Characteristic

4.2.1 Performance of power supplies

We must consider the condition of the supply voltage when we layout the RESET circuit. The switching performance of the AC/DC power supply in figure 3.33, depends on the switching point of the sine wave at the input. Therefore the load capacitor can be charged to different levels. The capacitor will be partly charged during the first half of the sine wave. Then the output voltage will show a drop over the time, as shown in figure 3.34. Therefore several periods of the AC voltage are necessary to stabilise the output voltage. For AC/DC power supplies the settling time needs to be approximately 10 ms. The SVS circuit must set the RESET– signal active until the power supply voltage is stabilised.

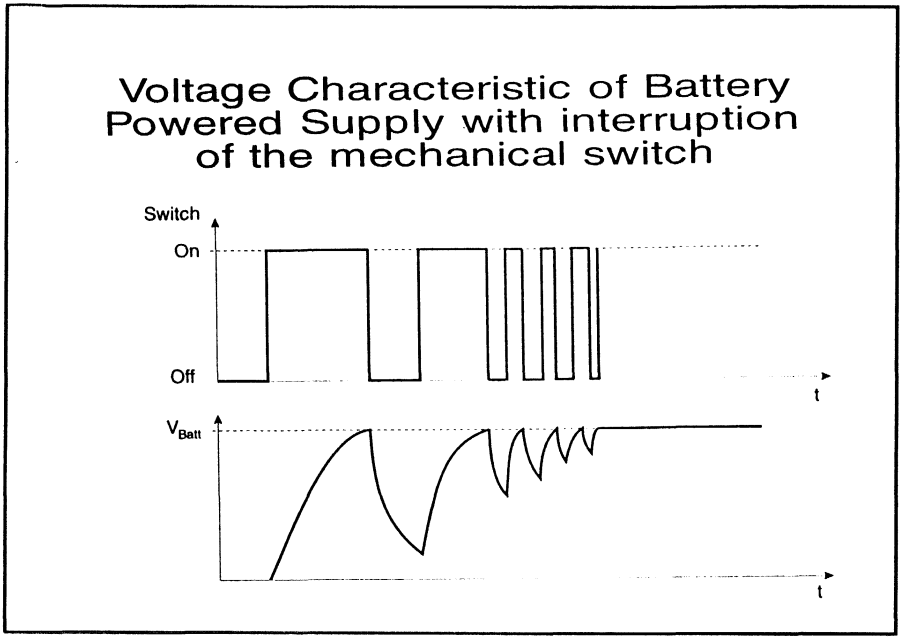


Figure 3.35 - Battery Supply Voltage Characteristic

Battery powered supplies have the advantage that the DC voltage level will be reached immediately after connection. However, a delay time arises from the conjunction of the blocking and filter capacitors and the internal resistance of the battery. For calculation we can use:

Ri = 0.1 to 10 Ohm and Cf = 10µF to 1000µF

To reach 95% of the nominal supply voltage, following equation will be useful:

$$0.95Vcc \rightarrow t = -Ri.Cf.\ln(0.05)$$

Therefore the rise time is between 0.03 and 30 ms.

Another factor is the interruption of a mechanical switch, which has also an impact on the rise time, see figure 3.35. The RESET circuit must be designed to keep the supervision circuit active until the supply voltage reaches its nominal value.

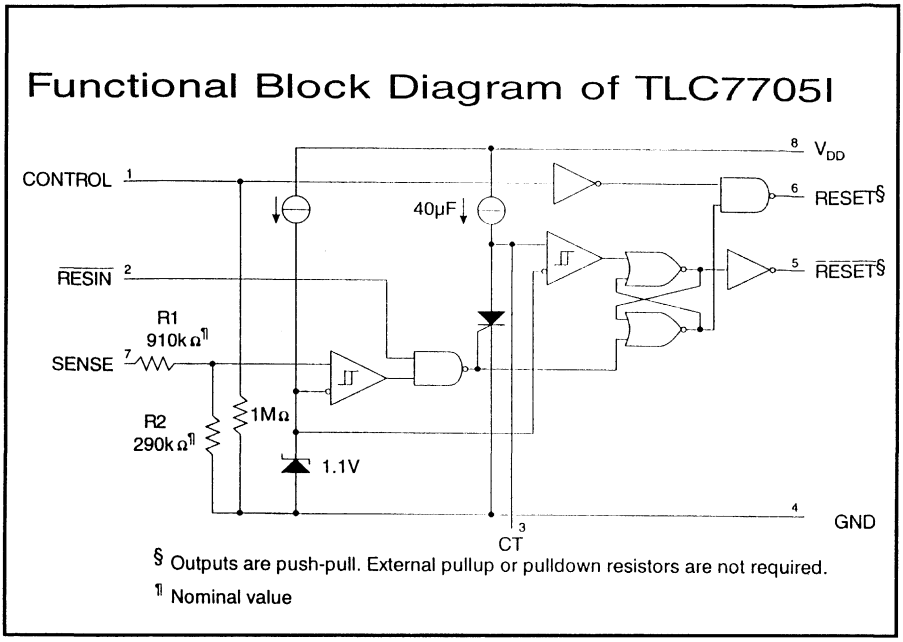


Figure 3.36 - TLC7705I Block Diagram

4.2.2 TLC7705 Product description

To meet the need for low power supply voltage, TI has released the TLC7705I. This is a low power enhancement of the industry standard TL7705A using the LinBiCMOS™ process and supervises 5-V supplies. This micropower supply voltage supervisor is designed for reset control in microprocessor systems. The functional block diagram is shown in figure 3.36.

At power-on, RESET is asserted when Vdd reaches 1 V. After the minimum Vdd is established, the circuit tests the SENSE voltage and keeps the reset outputs active as long as the SENSE voltage remains below the threshold voltage. An internal timer delays the return of the output to its inactive state to ensure proper system reset. The delay time td is determined by an external capacitor:

$$td = 2.1 \times 10^4 \times Ct$$

Ct in Farads, td in seconds.

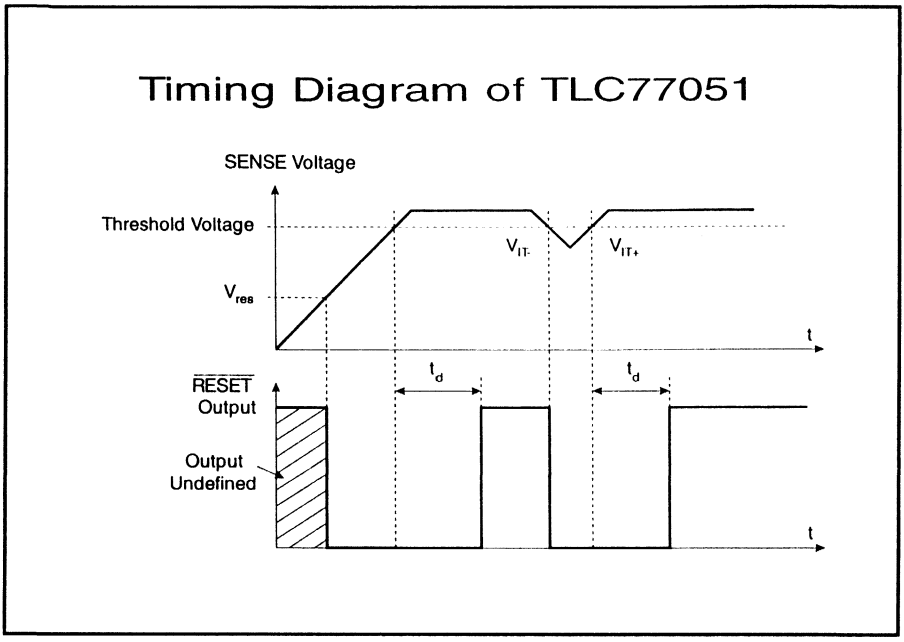


Figure 3.37 - TLC7705I Timing Diagram

When the SENSE voltage of the TLC7705I drops below the threshold voltage, the outputs become active and stay in that state until the SENSE voltage rises above the threshold voltage.

When CONTROL is tied to ground, RESET will act as active high. The supervision circuit contains additional logic for control of static memories with battery backup during power failure.

4.2.3 Design ideas

In order to achieve good system supervision we must understand the detailed performance and the switch-on time of the supervised circuit.

The delay time td is a function of the stabilised supply voltage of the supervised system. The system will be active when all parts of the circuit are functional.

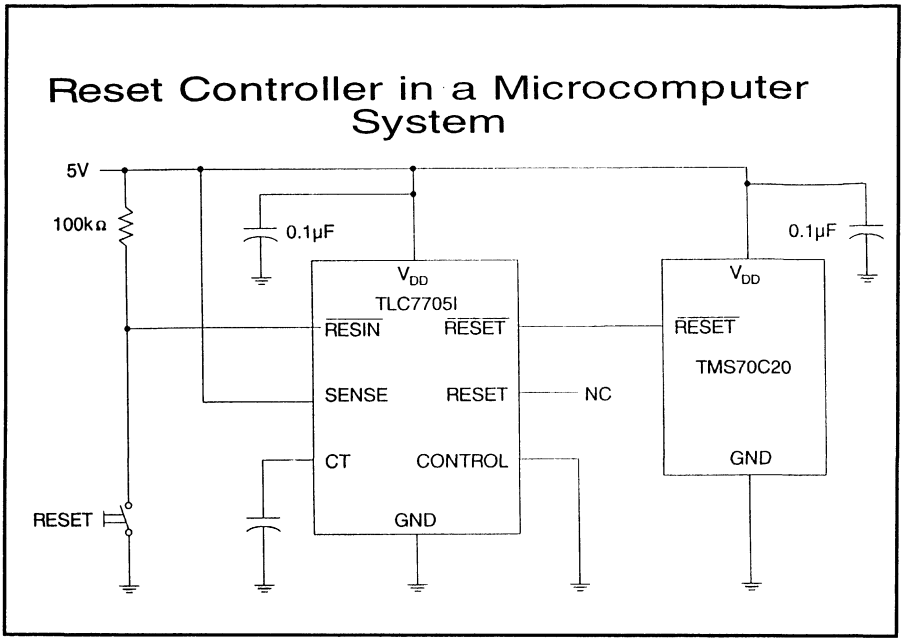


Figure 3.38 - TLC7705 as a Reset Controller

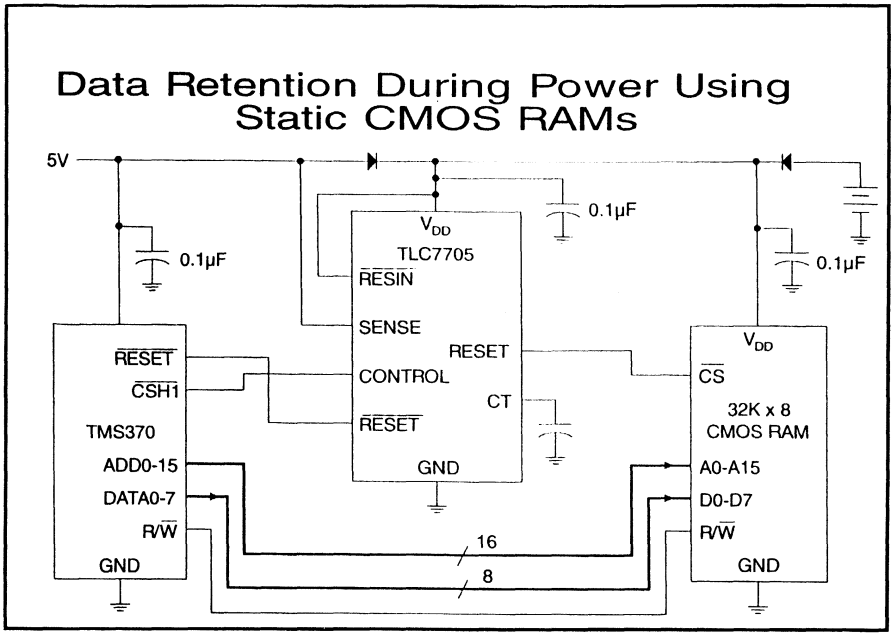


Figure 3.39 - SRAM Data Retention During Power-down

4.3 TL2218-285 SCSI terminator

The SCSI high-speed multi-point communication standard allows both single ended and differential transmission. Here we are concerned only with the single ended interface.

Single ended SCSI employs a driver and receiver configuration using TTL logic levels as shown in figure 3.40. It is primarily intended for applications within a cabinet, with the maximum line length being limited to 6 metres, and with up to 6 devices connected to the line.

Whereas EIA-232 had data rates of 20kbps, this single ended standard is intended for data rates between 1 and 5 million transfers per second (equivalent to 10 to 40 Mbytes/sec). The importance of termination in high speed multi-point communications is clearly demonstrated as innovative techniques are enabling the maximum transfer rate to approach 10 Mtps (80 Mbps).

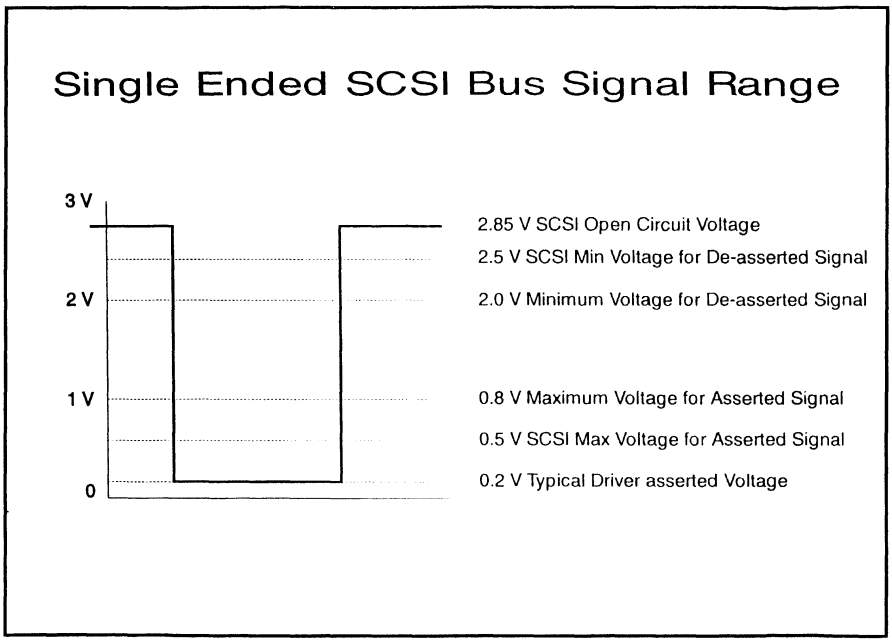


Figure 3.40 - Single-ended SCSI Bus Signal Range

4.3.1 Single ended SCSI termination

Proper termination of a bi-directional bus such as SCSI requires terminators at each end of the cable, with the terminator's job being to source as much current as possible during de-assertion. This is covered by the SCSI specification, which sets the limit for each terminator to a maximum supply of 24 mA. This prevents the line current from exceeding the 48 mA current sink limit of the open collector drivers.

The role of the SCSI terminator is not confined to low-to-high signal transitions. Once a signal has been de-asserted, the terminator is required to bias the bus lines to the correct open circuit voltage level, to ensure maximum noise margins.

Now we take a look at the two best known methods of single ended SCSI termination.

4.3.2 Passive and active SCSI termination

SCSI termination has traditionally been carried out using passive termination networks. As illustrated in figure 3.41, these consist of two resistors per signal line, one capacitor and a Schottky diode. This type of termination typically results in a maximum line current of approximately 17 mA. On a heavily loaded bus, the calculation gives a first step value of 1.76 V – well short of the desired 2.0 V level. As a result the line voltage will fluctuate with variations in the load current and TERMPWR. This leads to smaller noise margins, lower line currents and reduced data rates.

A better solution is active termination using a voltage regulator in series with a 100 Ohm resistor per line (figure 3.41). This method, known as active Boulay termination, was developed to overcome the main shortcomings of passive termination. The 110 Ohm resistor increases the typical line current available on de-assertion to 21 mA. This is equivalent to a 35% increase in line impedance, from the transmission line viewpoint. The line current and the high-level noise margins are also more stable since TERMPWR is no longer used to set the bias voltage directly, which is now done by the voltage regulator.

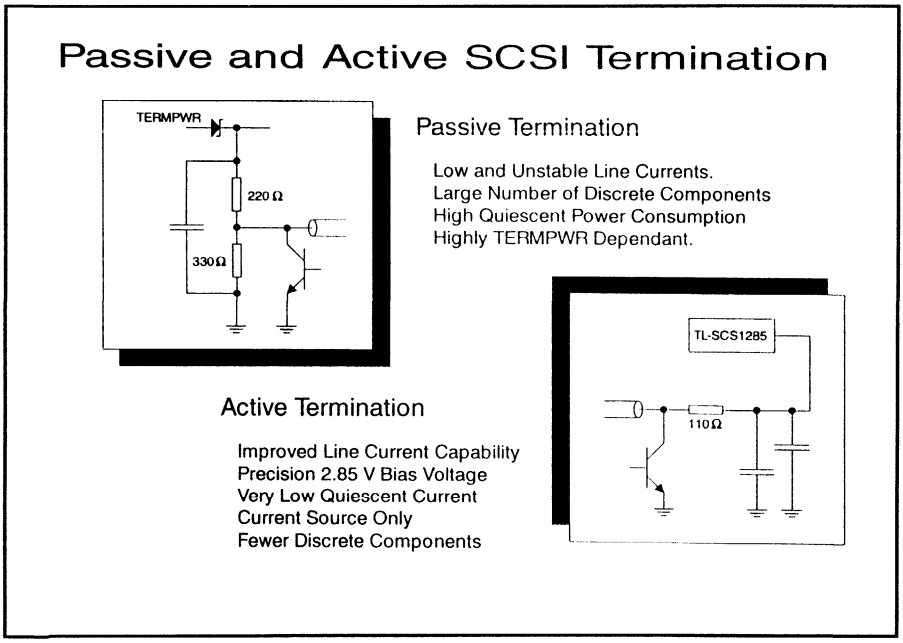


Figure 3.41 - Passive and Active SCSI Termination

4.3.3 Current source termination using the TL2218-285

Further improvements beyond active termination are achieved by the use of a current mode terminator. The TL2218-285 introduced by Texas Instruments is such a product.

The TL2218-285 current mode, or non-linear, device does not contain a voltage regulator. This means that no filtering or stabilising capacitors are needed, unlike 'completely integrated' active terminators. Another major difference between the TL2218-285 and passive and active terminators is that the current available on de-assertion is independent of the terminator voltage (figure 3.42).

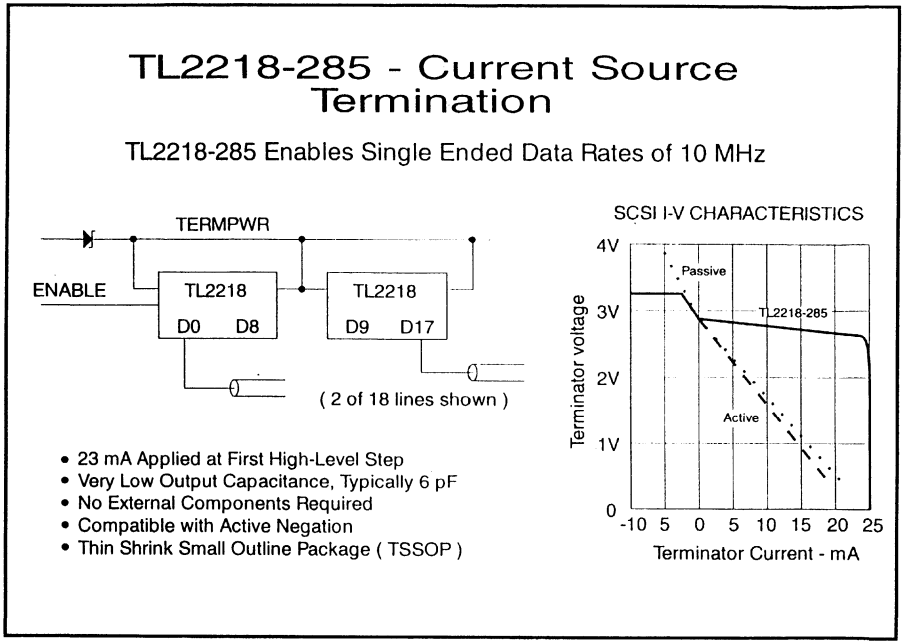


Figure 3.42 - Current Source Termination

During de-assertion the TL2218-285 operates as a 23.5 mA current source which is able to maintain this current level until the signal reaches the correct SCSI open circuit voltage. At this point the TL2218-285 becomes a voltage source of 2.85 V.

The additional current supplied by the device reduces the low-to-high transition time by ensuring that each voltage step is consistently the largest possible. The effect can be seen in Figure 3.43, which shows the signal waveforms obtained after using the TL2218-285 to terminate a 50 Ohm cable. Even at 10 MHz the first step voltage still exceeds the desired 2.0 V level.

Another feature of the TL2218-285 is the inclusion of a disable function which allows the terminator output to be shut down. This is particularly useful for a peripheral which finds itself somewhere other than at the physical end of the bus.

If disabled, the circuit consumes just 500 μA of current, and maintains an output capacitance of 6 pF. With the 15 pF typical output capacitance of a peripheral

transceiver, this will give a total node capacitance well within the 25 pF SCSI limit. A voltage terminator will normally maintain a disabled output capacitance of at least 10 pF, often leaving the system to operate outside the SCSI specification.

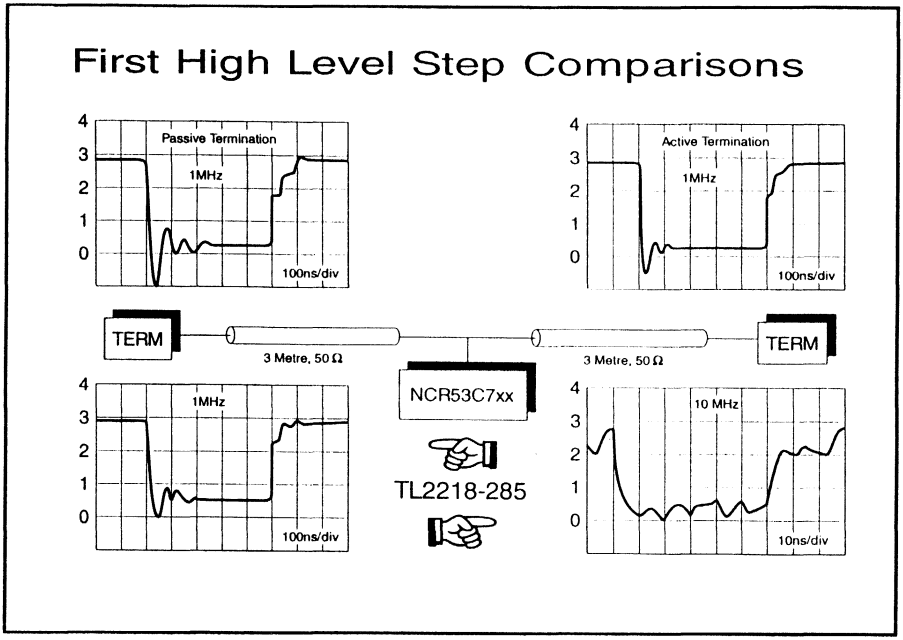


Figure 3.43 - SCSI Step Comparisons

A potentially damaging situation arises when active negation drivers are being used. These devices sense bus voltages and source sufficient additional current to ensure the first step voltage reaches the minimum SCSI level. Despite this attractive feature their relatively high cost has limited their use to ultra fast control lines such as ACK and REQ.

4.3.4 Power considerations

Although it increases the data rate, line termination will also increase the power consumption of a SCSI system. With the increased use of SCSI in portable or battery powered systems this is important.

During data on periods, the power dissipation on each of the SCSI termination methods is very similar. For an 8-bit bus with all the data lines asserted, the power dissipation in each case will be around 1 Watt.

During data off periods the position is significantly changed. The resistor dividers of a passive terminator will still draw around 750 mW of power. Both the TL2218-285 and active terminators, however, require a total quiescent current of less than 10 mA, providing a 30% saving in power consumption.

For a single TL2218-285 it is possible to calculate a worst case dynamic power dissipation of 493 mW. This assumes that all nine lines in the package are asserted simultaneously and experience a 50% duty cycle.

Battery powered systems also benefit from the extended TERMPWR range of the TL2218-285. Compared with competing solutions, which require a minimum TERMPWR of 4 Volts, the 3.5V to 5.5 V range of the TL2218-285 greatly increases the potential for prolonged operation.

4.4 TL7726 Clamp Circuit

The TL7726 voltage limiter has been designed to protect sensitive linear components in harsh industrial or automotive environments. One problem with most voltage clamps is that they will clamp the sensitive device they are trying to protect only when the input voltage has gone above the supply voltage by more than one diode voltage. The TL7726 was developed to overcome this problem. Normal protectors using bipolar or Schottky diodes will clamp only to within 400mV of the supply. The TL7726 clamp circuit can clamp within 200mV. The positive clamping voltage of the TL7726 is set by its reference voltage, which is normally tied to the supply voltage of the device it protects.

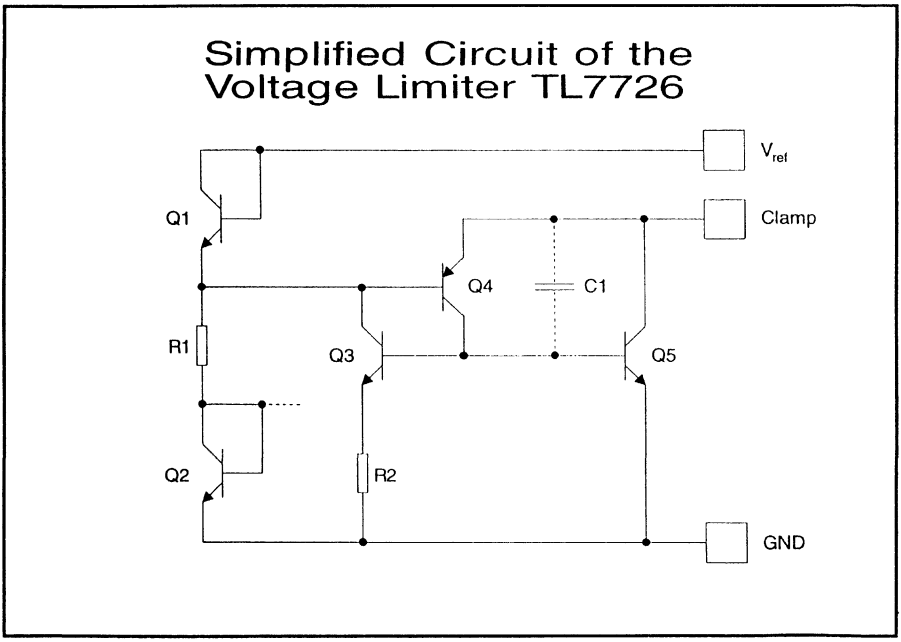


Figure 3.44 - TL7726 Simplified Circuit

The precision hex voltage limiter TL7726 has clamping diodes on chip with extremely low forward voltages. This circuit is shown in Figure3.44.

An internal reference voltage must be generated across the transistor Q1, connected as a diode; this internal reference is one diode forward voltage drop below the external Vref. The current through Q1, which is determined by the resistor R1, is only a few microamps. As a result, the supply rail of the circuit to be protected (usually connected to Vref) will be only very slightly loaded, allowing this voltage limiter to be used with

battery-powered equipment. The transistor Q2 generates a reference voltage, with a circuit complementary to that of Q1, which limits voltages more negative than GND.

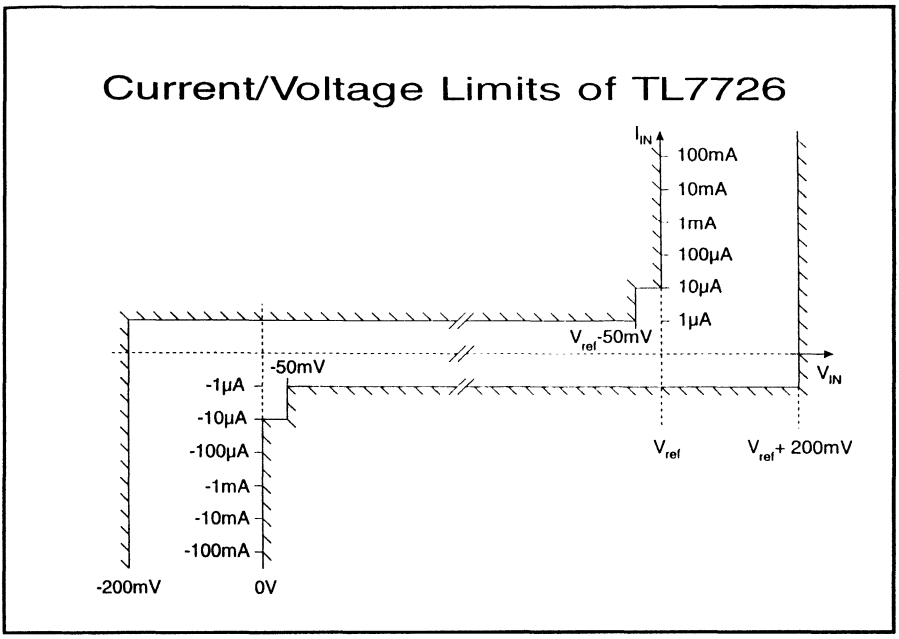


Figure 3.45 - TL7726 Current / Voltage Limits

The voltage to be limited is connected to the clamp input. If now the voltage at this point becomes more positive than the internal reference voltage at the emitter Q1, plus the foreward voltage of the base-emitter diode of Q4, then a collector current will flow in Q4. This current will come in part from base of Q3, whose collector current will then further increase the base current of Q4. This feedback ensures that the base current of Q5 and also its collector current simultaneously increase rapidly. This circuit technique ensures that a current of only a few microamps flows in Vref, so long as the voltage at the clamp input is the same as, or smaller than, the reference voltage Vref. A small increase of the voltage at the clamp terminal causes the current to increase very rapidly, see figure 3.45.

Fast operation of the TL7726 has been achieved with the capacitor C1 in figure 3.44 which essentially consists of the collector-base (Miller) capacitance of Q5.

An application of the TL7726 is shown in Figure 3.46. For an input voltage between ground and Vref, the clamping circuits present a very high impedance to GND, drawing current of less than 10µA. When the clamping circuits are in the active state for Vin<GND or Vin>Vref, they have a very low impedance and can sink up to 25mA. If the circuit needs to be protected against high voltages, external series resistors Rv will be needed. The resistor values can be chosen between tens of Ohms up to kOhms depending on the external input voltage.

The new TL7726 precision hex voltage limiter now provides, in a single SO-package, protection and reliable operation for up to six analogue channels.

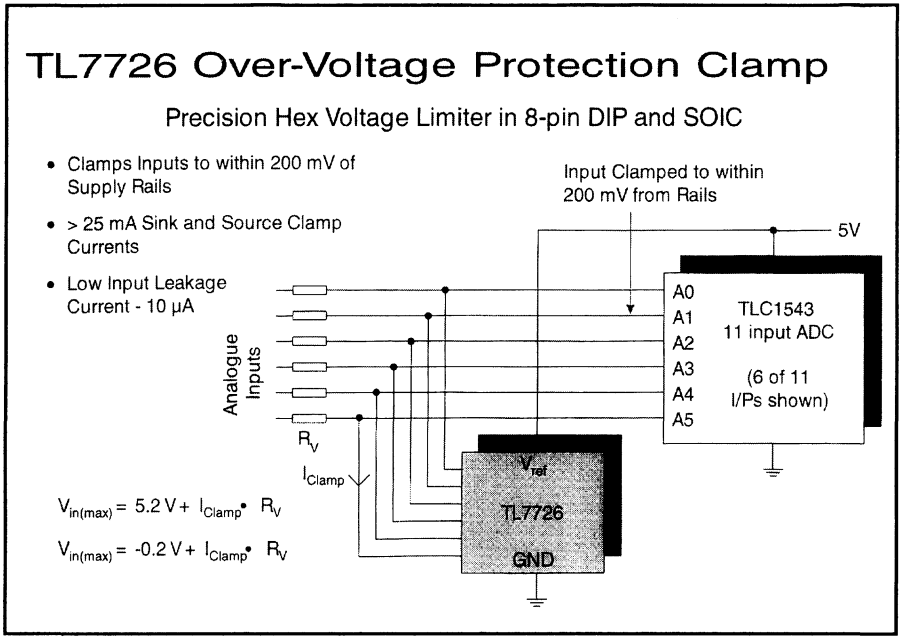


Figure 3.46 - TL7726 Application

Section 4
Power Drive Circuits

Section Contributions by:

David Cotton Julie Holland Mick Maytum
Ben Mullett Charles Wray
Jean-Claude Baumer

Contents Section 4

1 Introduction

1.1 Power+™ Spectrum

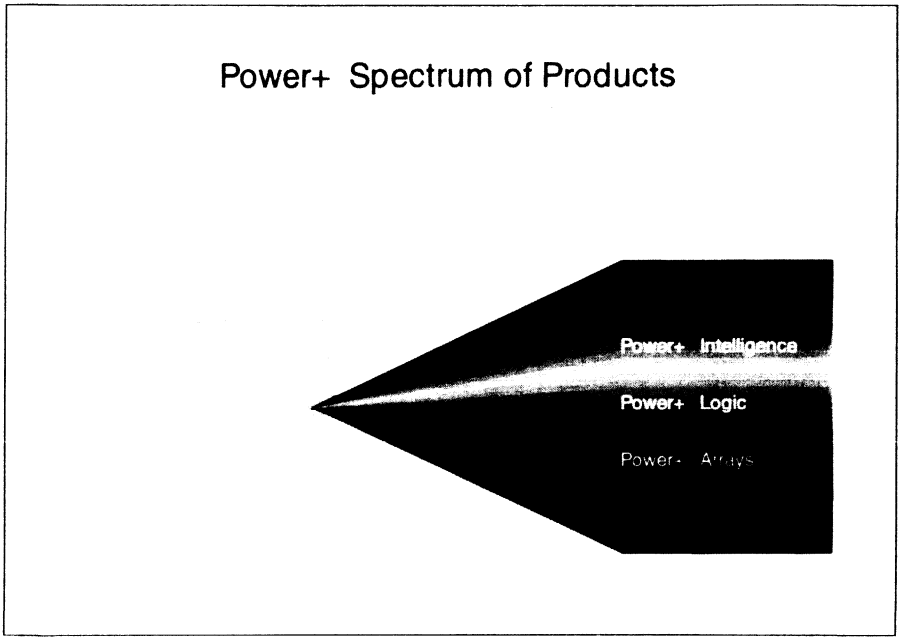


Figure 4.1.1 Power+™ Spectrum of Products

Texas Instruments Power+ Products are the latest in a series of power devices introduced by TI since the 1970s. The future growth path reflects the major strides made in recent months by our process engineers, and leads us to examine the process used in more detail.

1.2 Lateral DMOS

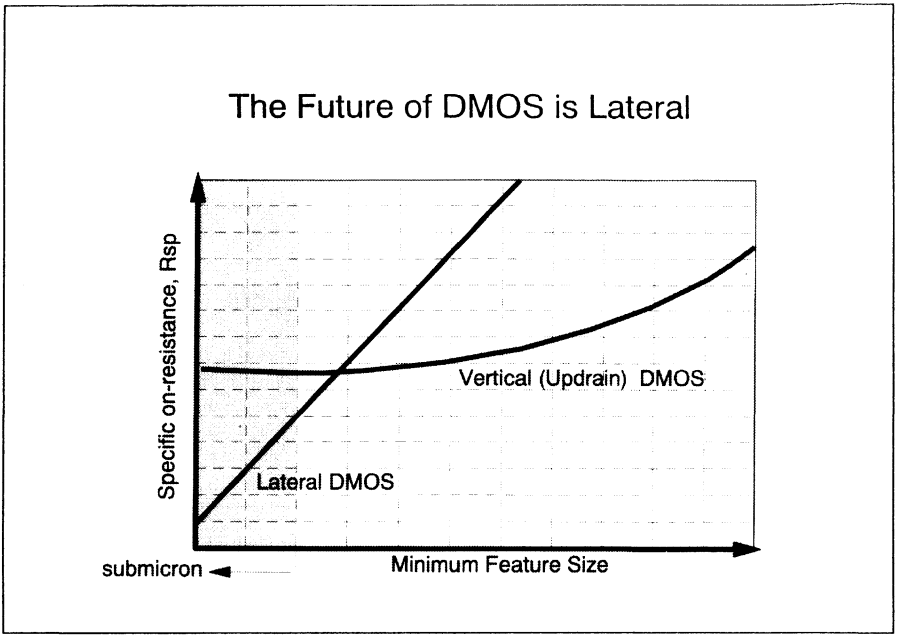


Figure 4.1.2 Lateral DMOS Performance vs. Vertical DMOS

The graph shows clearly the increasing perfomance advantage of Lateral DMOS (LDMOS) over conventional structures as feature size reduces. The graph is purposely vague in its terms, since processes vary. What is clear is that process-for-process, LDMOS is superior in the submicron region, which is where all manufacturers are headed, if they wish to remain cost-competitive. The impact of this technology advantage is only just starting to be felt, and will start to make its mark later this year.

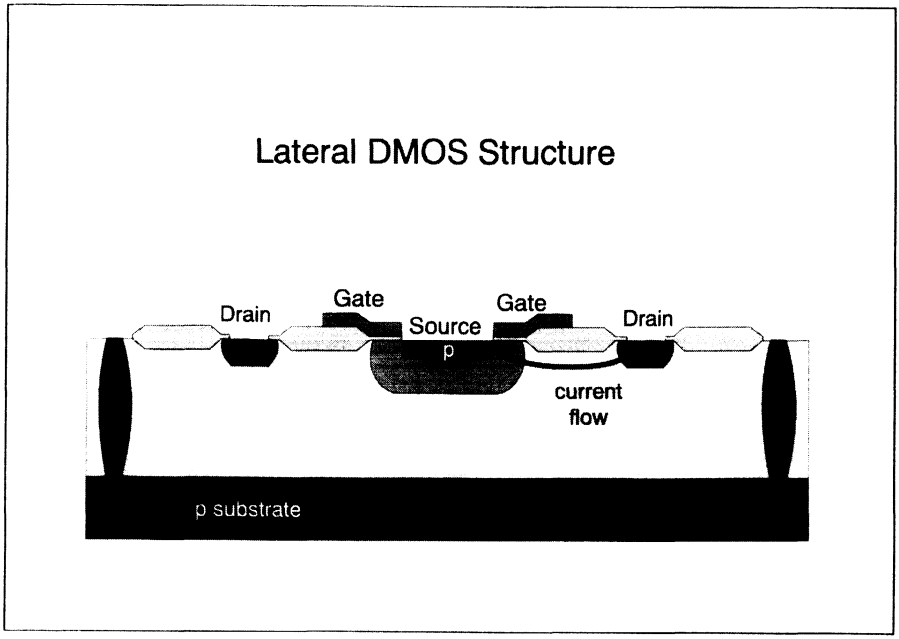


Figure 4.1.3 Lateral DMOS Cross Section

This section through an LDMOS FET shows the directness of the lateral current path compared with vertical or updrain DMOS. The design is also compact, which reduces the size of a given device, and thus reduces the cost of a given switch performance.

As feature sizes reduce with development, so the directness of the lateral current path improves, and the performance of the switch improves proportionally. With vertical or updrain DMOS, the vertical path(s) dominates the overall path length. This does not scale with feature size.

1.3 PRISM Methodology

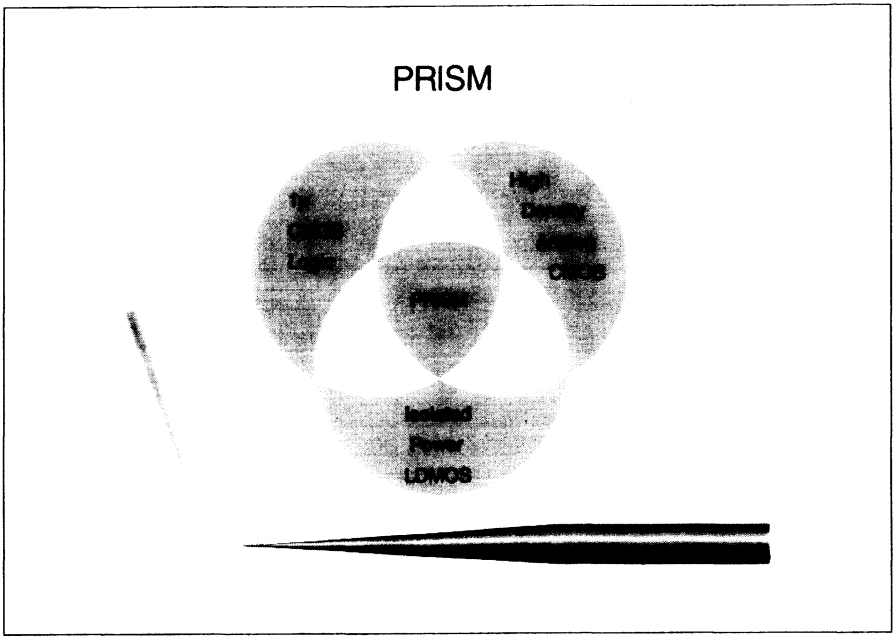


Figure 4.1.4 PRISM

PRISM is a mixed power, linear and logic process methodology that includes a Cell-based library for rapid design turnaround, analog and VLSI CMOS, EPROM and EEPROM, with LDMOS power capability.

The spread of process modules available ensures that the highest levels of integration are possible, and the specialisation ensures that there is minimum performance compromise. Examples are the EEPROM process in PRISM that can be combined with LDMOS power devices, logic and linear to build an EE-programmable power product.

The logic might comprise a microprocessor, a state machine or random logic, dependent on the application. The linear elements might involve op amps, comparators, charge pumps, regulators and FET drivers. Many of these functions are to be found inside the TPIC family of products.

1.4 Technology trends

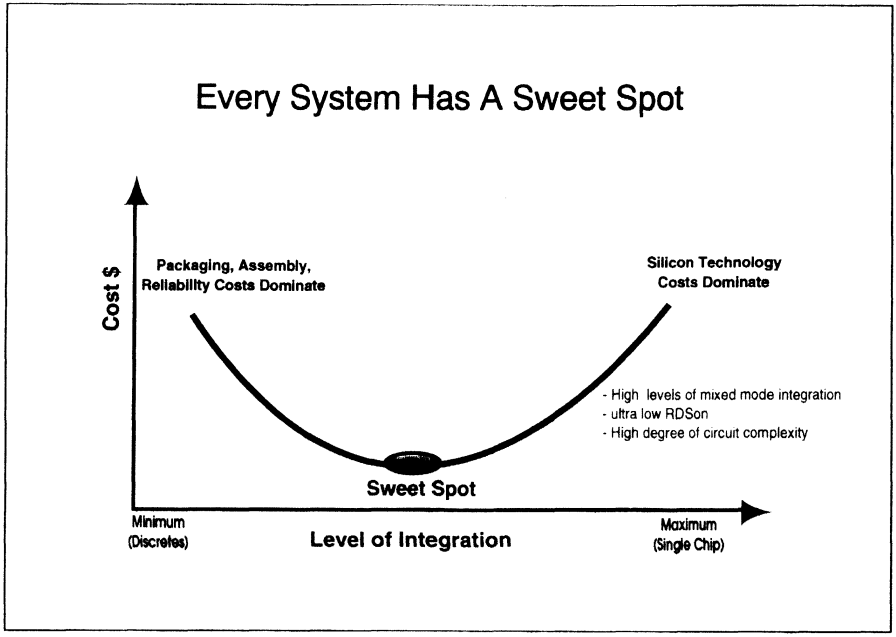


Figure 4.1.5 Finding the sweet spot

Often solutions to system problems cluster around a "sweet spot" where the trade-offs balance out to provide a good general solution. This is often the case with power and intelligent power ICs.

Successful power ICs tend to have output capabilities that are usually less than an amp or two, with the occasional exception. Higher currents are possible, and become more possible with time, but they rarely appear on highly integrated devices.

At the high integration end of the scale, discrete solutions can cost less than highly integrated ones which require complex fabrication processing. An example would be a 32-bit micro with an array of 20-Amp switches, EEPROM, an ADC, DAC, etc. All this is possible in PRISM, but it is probably cheaper today if the large switches are in an off-chip array.

At the low end of the integration scale, costs start to rise again as package count increases. To take an extreme example, no-one expects to build a standard op amp or NAND gate from discrete transistors. Another example would be an 8-pin op amp being replaced by a large number of 3-pin transistors, plus passives. This increases the interconnections and affects reliability adversely.

The most important point to be made here is that the "Sweet Spot" is NOT fixed. It moves with new developments, and with the acceptance of new solutions. In general silicon technology improvements result in smaller physical size, and this will in time favour higher integration.

As a result of recent process innovations, the "sweet Spot" for Power+™ ICs is moving away from the traditional 1 or 2 Amp products with minimal integration, and it is moving in two directions.

The first direction is the obvious one – higher current, higher integration and lower on-resistance are continuing goals – but the way they have been achieved brings lower specific on-resistance to all devices.

Thus the size and dissipation of smaller devices is reduced proportionally. They become better able to be associated with greater amounts of logic, and to be available in smaller packages – e.g. surface mount, and specifically SO packages. This means that new product families will be appearing at both ends of the power spectrum.

1.5 Power+ Products

Due to the "Sweet Spot" in figure 4.1.5, TI offers three levels of partitioning:

Power+ Array™ : Integration of multiple DMOS power switches in different configurations

Power+ Logic™ : Integration of high speed CMOS Input Logic with DMOS power switches

Power+ Intelligence : Integration of protection and diagnosis capability together with CMOS Logic and DMOS power switches

Higher levels of integration tend to cause customization. This means that Power+ Intelligence is often targetted to special markets. Figure 4.1.6 illustrates the increasing customization due to the higher level of integration.

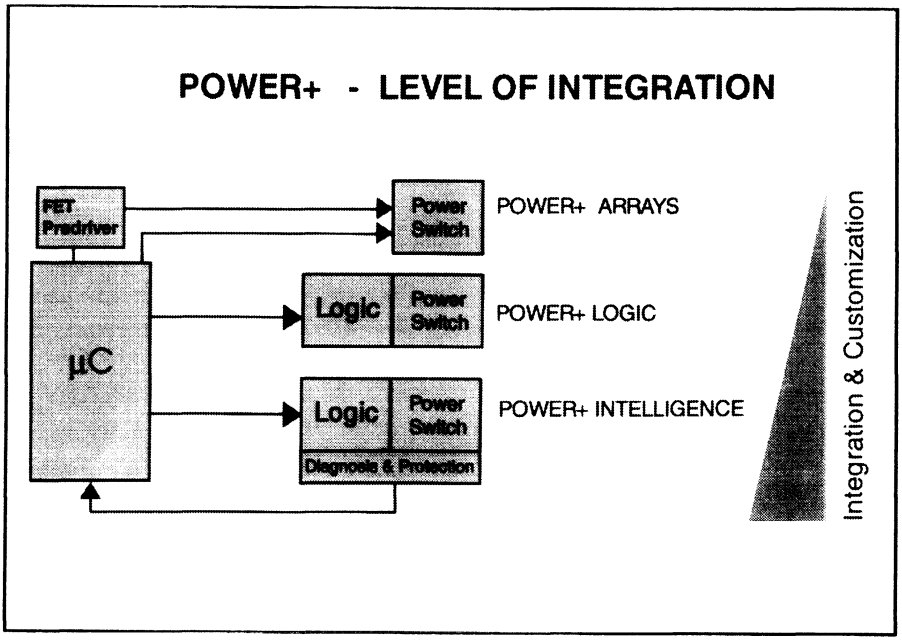


Figure 4.1.6 Level of Integration

The highest conceivable level of integration might be a power switching configuration with a microprocessor. How far power switching systems should be integrated is a question of cost, not of technology.

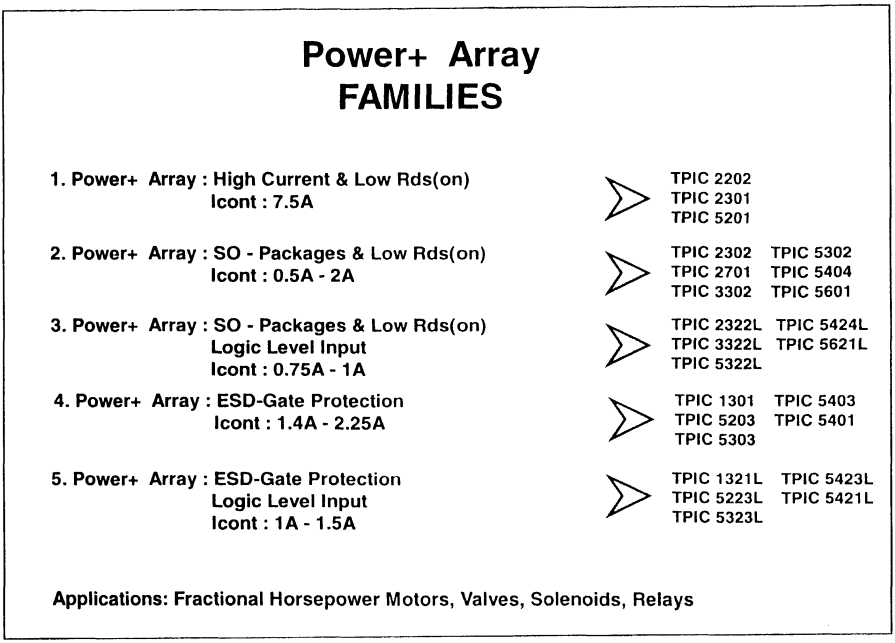


Figure 4.1.7 Power+ Array Family

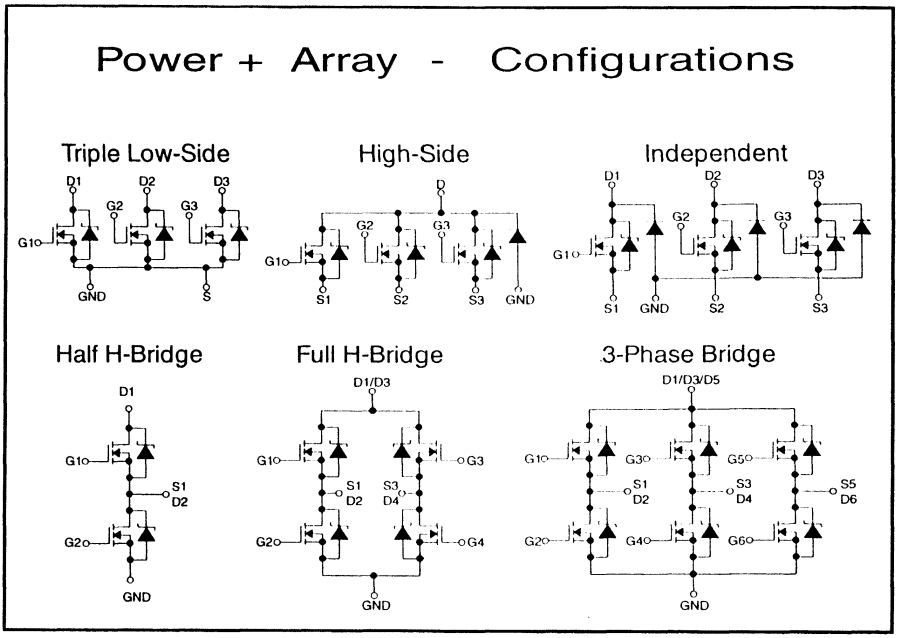


Figure 4.1.8 Power+ Array Configurations

Here the Power+ Array family is shown in brief. These devices are monolithic configurations of LDMOS switches in single packages. Figure 4.1.7 summarises the differences between the families. The first group is characterized by high current capability; the second by the small SO-package and the low $R_{DS(on)}$. The third group has similar configurations to the second, but allows standard 5V logic input to drive the arrays. The 4th and 5th group offer 4kV ESD input protection by integration of two zener diodes. This gives a high protection which is well-suited for ESD-sensitve and noise-intensive applications. The 5th group permits logic level inputs.

The TO220 arrays of group 1 offer 90 mOhm switching at the voltages and currents shown. The two Dual devices, the TPIC2202 (common-source) and the TPIC5201 (separate devices) offer a choice when (e.g.) building H-bridge configurations. These are shown later in the applications sections. The TPIC2301 is a Triple common-source device in the same 7-lead TO220 package as the TPIC5201.

Group 2 of Power+ Arrays are robust 0.3/0.5 Ohm DMOS switches with a maximum output voltage of 60V and guaranteed avalanche energy capability to support predictable designs of inductive load switches.

The TPIC2701 is a Sept (7 FETs) device with common sources and an output clamp pin. Its current capability is less than the TO-220 arrays, but it is considerably greater than the ULN200x series with which it is pin compatible. It offers higher current capability over the same temperature range, better dissipation, and a specification that extends to 125°C as opposed to 85°C.

The avalanche energy value (22 mJoules) encourages its use in inductor driver design due to its guaranteed switch-off capability. This can help prevent the type of mysterious occasional failures experienced with bipolar arrays when used without adequate snubbing networks, or it can reduce snubbing network costs.

The TPIC2302 is a triple low side driver array. It has current ratings per channel of 1A continuous, 5A peak. Each output can absorb 24mJ avalanche energy. The TPIC2302 is particularly suitable for 3-phase brushless DC motors. The TPIC3302 has the same switch performance, but is configured as a high-side array. The TPIC2302 and 3302 are offered in a 8-pin SO-package.

The TPIC5302 is a monolithic configuration of 3 independent switches in the 16-pin SO package. Each channel is rated at 1.4A continuous, 7A peak. Each channel can absorb 13.6mJ avalanche energy.

The TPIC5404 is configured as a full H-bridge. The TPIC5404 is offered in either 16-pin DIP or 20-pin SO packages. It is very robust, rated at 2A (1.7A in SO package) continuous and 10A peak current per channel. Each channel can absorb 21mJ of avalanche energy, making it well-suited for a wide range of fractional horsepower motors.

The TPIC5601 contains six switches configured as a 3-phase bridge driver. Current ratings are 1.7A continuous, 8A peak, per channel. The avalanche energy rating of each channel is 21mJ. It is available in the 20-pin SO package.

Group 3 of Power+ Arrays expands the Power+ portfolio by monolithic logic level power DMOS arrays. These offer a logic level gate drive and therefore interface directly to standard 5V level predrivers. The advantage to drive the gate with a lower voltage level results in a lower continuous current capability, the TPIC2322L and the TPIC3322L have 0.75A (2.25A peak), the TPIC5322L with 1A (3A peak) and at least the TPIC5424L and the TPIC5621L with 1a (3A peak).

The TPICxxxxL ('L' means logic drive) devices provide a range of rugged 0.4 to 0.6 Ohm power DMOS switches in the space efficient package with similiar configurations to group 2.

To offer a solution for ESD sensitive and noise intensive applications, including fractional horse power motors in various office end equipment and industrial systems, Texas Instruments introduces gate protected motor drivers. All of these Power+ Arrays feature integrated high current 18V zener diodes to help prevent gate damage in the the event of a voltage transient. These zener diodes are tested using the human-body model of a 100pF capacitor in series with a 1.5kOhm resistor. This configuration enables a specification of 4000V ESD protection.

The combination of integrated gate-source zener diodes and energy rated drain-source zener diodes provides improved reliability against operating and static-induced voltage spikes.

The logic level versions with gate protection are available in the equivalent DMOS-transistor configurations. The logic level interfaces directly to the 5V standard logic level and offers therefore a high level of flexibility and simplifies the predrive circuitry.

The TPIC5203 / TPIC5223L (= Logic Level Input) are built with a gate-protected independent pair of Power-DMOS switches of 1.6A / 1A continuous, 8A / 3A peak current capability per channel. The avalanche energy capabilty is guaranteed at 21.6mJ/108mJ. This configuration is offered in an 8-pin SO package.

The TPIC5303 / TPIC5323L is a triple gate-protected independent driver. Each channel is rated at 1.4A / 1A continuous and 5A / 3A peak current and a guaranteed anvalanche energy capability at 10.2mJ / 22.5mJ. The TPIC5303 / 5323L are offered in a 16-pin SO package.

The TPIC5403 / TPIC5423L offer four gate protected electrically isolated independent channels. They have current ratings of 2.25A / 1.25A continuous and 11.25A / 4A peak. Each output can absorb 17.2mJ / 96mJ avalanche energy. Both devices are available in the 24-pin wide-body SO package.

Well-suited for 3-phase bridge DC brushless motor applications are the TPIC1301 / TPIC1321L, gate-protected DMOS-transistors in a 3-Half H-bridge configuration. Each rugged DMOS output is rated at 2.25A / 1.25A continuous and 11.25A / 4A peak current and guarantees 17.2mJ / 96mJ avalanche energy capability. It is available in the 24-pin wide-body SO package.

The TPIC5401 / TPIC5421L is configured as a gate-protected full H-Bridge. Current ratings are either 2A / 1.5A continuous and 10A / 3A peak current in the 16-pin DIP package or 1.7A / 1A continuous current in the 20-pin wide-body SO package. The avalanche energy rating of each channel is 21mJ / 180mJ.

All outputs of the gate-protected generation are specified at a 60V output clamp voltage for switching high power loads. The temperature range is from -40 degrees C up to 125 degrees C. The low $R_{DS(on)}$ range of 0.26 Ohm to 0.6 Ohm minimizes power dissipation.

Power+ Logic FAMILIES

8 rugged DMOS power lowside switches
Integrated input CMOS logic
Current limit protection
Low Rds (on)
Guaranteed avalanche energy capability
Surface-Mount or Dual-Inline Package

Logic	Power configuration		
Addressable latch (TPICxx273)	6xxx	Standard	250mA
Octal D_Type latch (TPICxx259)	6Axxx	PWM current limit	350mA
Octal SIPO/shift reg. (TPICxx595)	6Bxxx	Soft current limit	150mA

Applications: Lamp arrays, Stepper Motors, valves, solenoids, relays

Figure 4.1.9 Power+ Logic Family

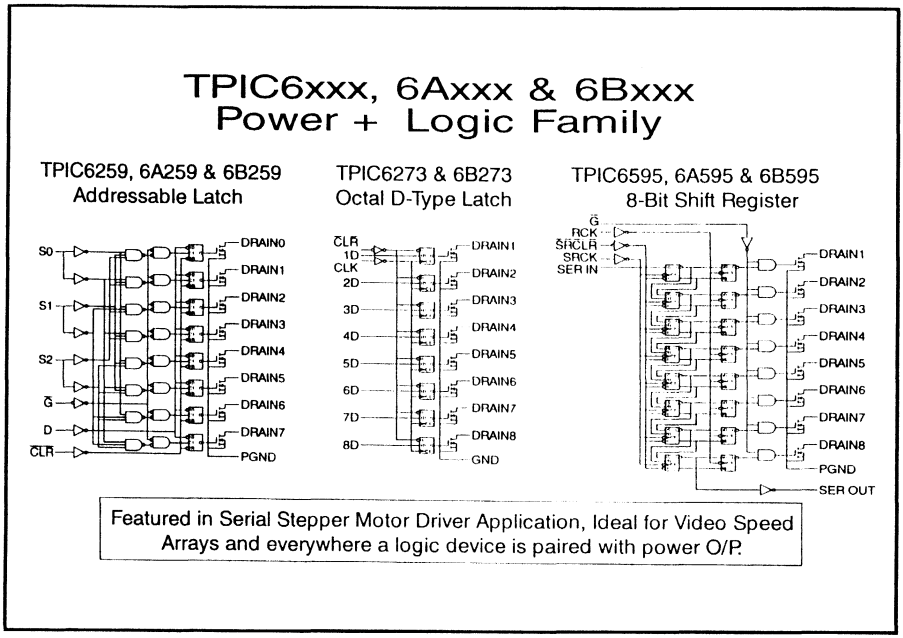


Figure 4.1.10 - Power+ Logic Common Logic Diagram

1.5.2 Power+ Logic

The Power+ Logic family contains multiple rugged DMOS power switches with high speed logic drivers. The nomenclature is as standard HC logic families (74xxx series). The integrated CMOS-logic configurations are a shift register (SIPO), a parallel latch and a 8-bit addressable latch. The input logic is as the part number suffix suggests, and the outputs are common lowside connected LDMOS FETs. There is current limiting on the enhanced 6Axxx parts and a soft current limit on the 6Bxxx family. The continuous current specification is shown in figure 4.1.9.

With their high speed CMOS input logic and the feasibility of cascading long chains, the serial parts are particularly effective in driving large arrays for displays; the shift register architecture minimises interconnects when driving large banks of LEDs, lamps or mechanical flippers in (e.g.) airport departure/arrival display systems. Operations up to 25 MHz are supported by the Power+ Logic family and make applications with high PWM resolutions or visual displays with video speeds possible.

The 6Axxx parts are particularly useful when driving incandescent lamps, since their current limiting extends the life of the lamps as well as protecting the device against short circuits. The 6Bxxx also has a peak load current specification at 500 mA per output, to prevent high inrush currents from the load.

Problems caused by driving loads (e.g. stepper motors) are well solved by the specified avalanche energy capability. This gives the advantage of saving external clamp diodes and/or snubber networks in systems.

The low $R_{DS(on)}$ provides a low power dissipation, hence the high density allows assembly in 20-pin surface mount packages, as well as the standard 20-pin DIP.

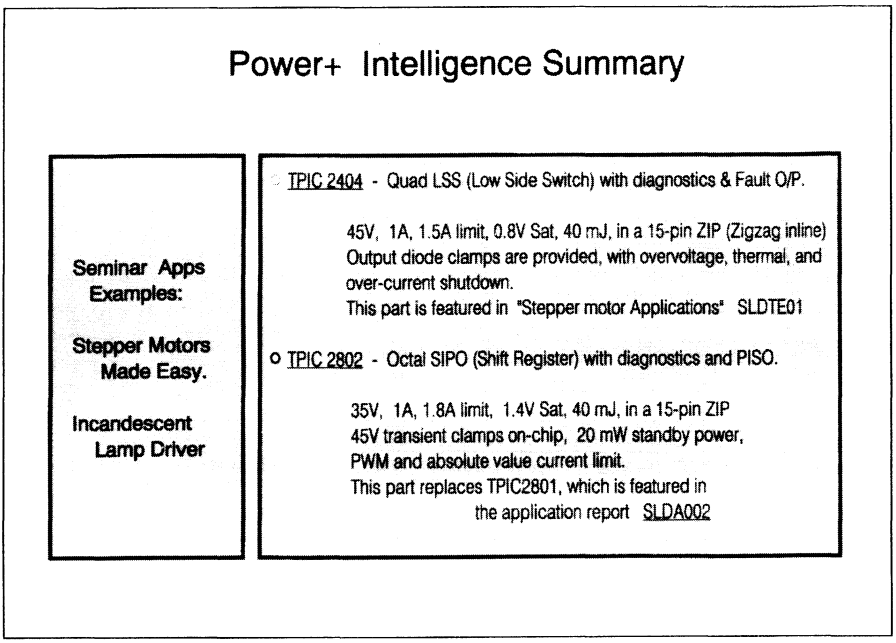


Figure 4.1.11 Power+ Intelligence

1.5.3 Power+ Intelligence

The Intelligence part of the "Power+ Intelligence" family reflects the ability of the device to sense the state of its power outputs, report faults, and feed data back to the controlling micro, logic system, or ASIC. This can save large amounts of external circuitry.

The TPIC 2404 is a useful output device with logic level inputs, and individual current and thermal limits on the outputs that turn off the drivers and signal a fault. Exceeding the overvoltage limit will also turn off the outputs and enable the fault output, as will open load/short to ground. Using the truth table on the data sheet, full output diagnostics can be carried out by toggling the inputs and reading the data output.

The TPIC 2802 replaces the popular TPIC 2801, its darlington outputs giving improved gain, and reducing current consumption as a result. The SIPO (Serial In Parallel Out) architecture is extended to allow PISO output readback from the serial out pin; this enables the output states to be interrogated remotely. Output protection includes a current limit with both PWM and absolute peak limits, and out-of-saturation voltage protection.

As mentioned earlier, increase of integration level generates a full feature set. Therefore Power+ Intelligence is targetted to customized products. For instance one family comprises full H-bridges with the integration of a complete protection- and diagnosis-

system. These products are specified to drive fractional horsepower motors in specific customer systems in the automotive sector.

2 Output System Design

2.1 Selecting a load device

This involves defining the type of output energy needed and selecting the correct size and class of load.

The next step is evaluation of the input requirements that address the voltage and current requirements during normal operation. Normal operation includes load switching (turn on, turn off and accompanying transients).

Often the behaviour of a load during switching is not adequately specified by the manufacturer and must be characterized for the specific application. This implies evaluating the system under operating conditions, examining the load behaviour, and then redesigning if necessary.

It cannot be stressed too highly that the approximations and rules of thumb that work for small signal devices do not always work in a power system. Current can be found flowing the "Wrong" way – especially in inductive circuits. Inductive portions can be found in many nominally resistive power circuits. This is due to the high currents, or high dI/dT appearing in (e.g.) the ground leads, generating unwanted ground offsets. It is recommended strongly that an oscilloscope be used to view the dynamic conditions of both voltage and current through the switch, and that this be used to inform any redesign.

2.1.1 Resistive loads, Capacitive loads and Inductive loads

Resistive loads are simplest, since sizing is largely a question of examining the current and voltage specification, estimating dissipation, making allowance for duty cycle, then allowing margins for safety. It is always worth checking the load for unsuspected inductive and capacitive components.

Incandescent lamps however, have a rapid initial current surge that reduces with time. These loads need care to ensure that the peak current is less than the switch limit – or a switch that provides its own current limit.

Current Limit can be more economical in many cases than just using an "overkill" device, since an incandescent lamp bulb may peak at 4A, before settling to 1A nominal. A 4A MOSFET is likely to be 4 times the area of a 1A MOSFET, with consequent cost increase, when a protected 1A device is adequate to the task, substantially smaller and therefore cheaper to make, and increases the life of the bulb.

Capacitive loads are comparatively rare - often stray capacitance is the only capacitive element in an otherwise resistive load. Where they are encountered, the principal danger arises from the high initial current into the (initially $\rightarrow \varnothing$ Ohms) load, which must be limited in some way if the switch is not to suffer – a switch with current limit is ideal.

Inductive loads can be complex to deal with, and energy can be passed from switch to load and back again to the switch. This energy must then be dissipated without damage, and a well-specified avalanche energy value for the switch device is helpful here.

Inductive loads usually have a significant resistive (and a small capacitive) component as well. Care must be taken to ensure that the energy return is fully understood and dealt with at the design (or re-design) phase. It is therefore important when driving inductive loads to use devices whose avalanche energy is fully specified, or to use other methods of protection such as snubbers, diode or zener diode clamps.

In the latter case, it can be beneficial to clamp to a voltage higher than the supply voltage, but lower than the specified device voltage; the higher voltage spike is usually of shorter duration, and therefore has less energy to dissipate, which means cooler running.

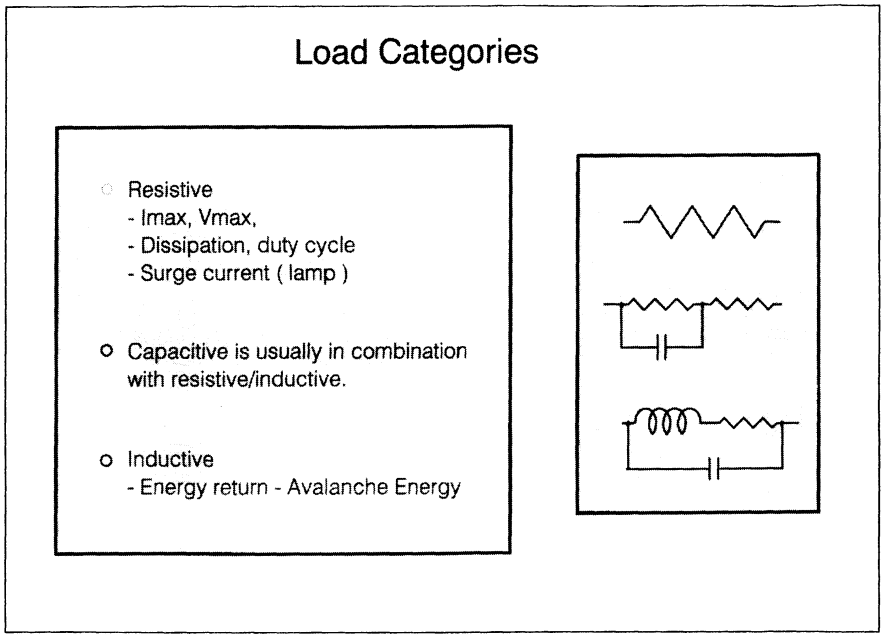


Figure 4.2.1 Categories of Load

2.2 Interface Circuit Requirements

If we assume that the interface circuit is a switch then what do we need to know in order to select the right switch?

Motors, solenoids, lamps and other assorted loads are generally specified by operating voltage and current. The information provided is sufficient for operating at continuous duty. However, in most applications the load is being switched on and off. When switching loads the operating requirements as well as transient conditions must be considered. The power requirements are often further influenced by dynamic operating conditions.

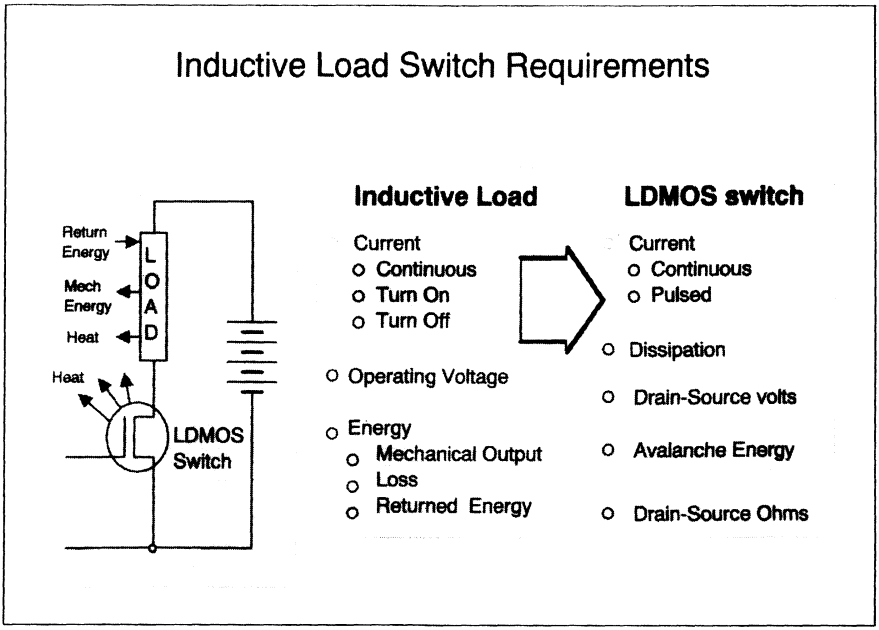


Figure 4.2.2 Inductive Load Switch Requirements

The easiest way to look at load requirements is to consider the example in Figure 4.2.2, of a load operating from a battery and controlled by a low side switch. What is needed to design the switch and evaluate the system?

The system power supply and load choice will determine:

- Current drawn from the battery, including transients when the switch is turned on and off.
- Battery terminal voltage. (V)
- Energy output from the load (motion, sound, etc.)
- Energy dissipated from the load in the form of heat. (IR loss, magnetic loss, friction)
- Energy returned to system (inductive, regeneration, cross coupling)

These system load requirements must then be used to determine the switch requirements:

- Continuous source-drain current
- Pulsed drain current
- Continuous power dissipation @ $T_A = 25°C$
- Single-pulse avalanche energy (energy returned to the switch from back e.m.f.)
- Drain-source voltage (V_{DS})
- Drain-source on-state resistance ($R_{DS(on)}$)

Selecting or designing a switch is a three step process:

- Determine the total energy, current and voltage required
- Select a switching device which will accommodate the energy
- Evaluate the system power dissipation to determine any heat sinking requirements.

2.3 Determining the Total Energy

This begins with evaluating the load current during operation and during switching.

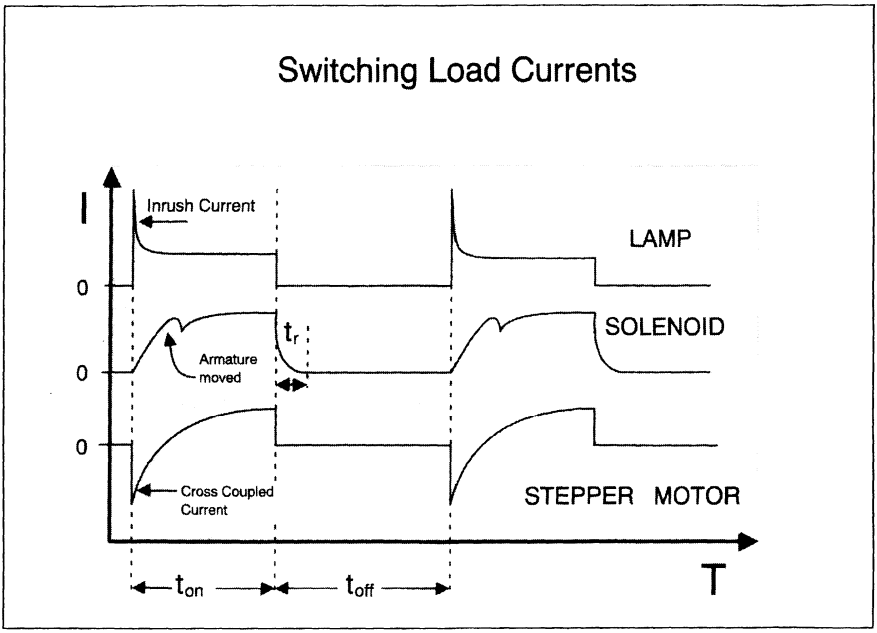


Figure 4.2.3 Switching Load Currents

Figure 4.2.3 shows the current waveforms for an incandescent lamp, a solenoid and a stepper motor. This diagram depicts steady state and switching conditions which must be considered in controlling a load.

The incandescent lamp current shows a high inrush value at turn on, (t_{on}) due to the difference in filament resistance when cold and hot, decreasing to a steady current value until turn off (t_{off}), and then a clean turn off with no current flowing after t_{off}.

A lamp control switch will need to withstand high peak currents or limit the current until the lamp filament warms up. The latter approach is preferable, since it extends the life of the filament.

The solenoid current starts at t_{on}, increases until t_{off}, and continues to flow until t_R. The change in current slope between t_{on} and t_{off} is caused by the solenoid armature moving closer to the coil and increasing the coil inductance. The current flow between t_{off}

and t_R is a result of the magnetic field in the solenoid collapsing and returning energy to the system.

A solenoid switch must be capable of conducting the coil operating current and the system must provide a method for accommodating the energy returned to the system at turn off. Several methods are employed to deal with the returned energy, which when it is dissipated in the switch is referred to as avalanche energy.

The stepper motor exhibits a exponential current increase characteristic of an inductive load. Return energy is a factor in stepper motor control. Additionally stepper motor windings can produce currents as a result of cross coupling from adjacent motor windings; this is particularly true for unipolar stepper motors. A control circuit for a stepper motor such as depicted in Figure 4.2.3 must accommodate the transient energy at turn on and the returned energy at turn off.

Once the load characteristics are determined energy calculations can proceed.

Energy and Power Calculations for an Inductive Load

- Power - on time MOSFET dissipation

$$P_{on} = \frac{1}{3}(I_p^2)\, r_{DS(on)}\, d$$

For $\frac{L}{R} >> t_{on}$

- Back emf energy

$$E_T = \frac{3 L I_p^2 V_{CL}}{6 (V_{CL} - V_{SS}) + 4 R_L I_{DM}}$$

- Power off dissipation

$$P_{off} = E_T f$$

- Total average switch power dissipation

$$P_T = (P_{on} + P_{off})n + P_{(quies)}$$

L	=	Load Inductance
I_p	=	Peak Drain Current
V_{CL}	=	Max O/P Clamp Voltage
V_{SS}	=	Load Supply voltage
R_L	=	Inductor Resistance
f	=	Switching frequency
d	=	Duty Cycle
$r_{DS(on)}$	=	Drain to Source Resistance
n	=	Number of switches Operating
$P_{(quies)}$	=	Quiescent Disipation of Switch
t_{on}	=	Switch On Time

Figure 4.2.4 Energy and Power Calculations for Inductive Loads

The energy calculations for an inductive load are presented in Figure 4.2.4. The intent is to calculate the total power dissipated in the transistor switch.

Power dissipated during switch "on" time is calculated as follows:

During the power-on time the inductor's current approximates to a linear ramp, assuming the inductors L/R_L time constant is much greater than the turn on time (t_{on}).

This results in a mean square drain current of 1/3 I_P^2 with I_P equal to the peak drain current. Therefore the average power dissipated in the output MOSFET, P_{on}, is equal to:

$P_{on(av)} = 1/3\ (I_P^2)^* R_{DS(on)} * d$

This assumption would be applicable to the stepper motor waveform in figure 4.2.3, but would not work for the solenoid. The solenoid time constant L/R_L is less than t_{on}, therefore P_{on} will be greater than that calculated above.

Power dissipated during switch off time is calculated as follows:

When the output MOSFET is turned off, the back e.m.f. generated by the inductor raises the drain voltage, which must be clamped either externally or internally. External clamping is normally accomplished with a snubber diode. Internal clamping is also accomplished with a zener diode; the clamp voltage V_{CL} is also called the avalanche voltage.

The equation to define avalanche energy is:

$E_T = (3 * L_H * I_P^2 * V_{CL})/(6 * (V_{CL} - V_{SS}) + 4 * R_L * I_P)$ .. JEDEC Standard No. 10;

This equation assumes a linear decay of the current in the inductor. A more accurate calculation of E_T can be derived by integrating the inductor current and clamp voltage in the load from turn off until the inductor current decays to zero as follows:

$$E_T = \int_0^{t_1} V_{CL} * I_L * dt;$$

$$I_L = (I_P + (V_{CL} - V_{SS})/R_L)\ e^{-(R_L/L)t} - (V_{CL} - V_{SS})/R_L;$$

$$I_P = V_{SS}/R_L\ (1 - e^{-(R_L/L_H * d/f)});$$

$$t_1 = L/R_L * \ln[1 + (I_P * R_L/(V_{CL} - V_{SS}))]$$

$$E_T = V_{CL} * L_H/R_L * (I_P - (V_{CL} - V_{SS})/R_L * \ln(1 + (I_P * R_L)/(V_{CL} - V_{SS}))$$

The power dissipated during the turn-off period, P_{off}, can be equated to the product of E_T and the frequency of switching

$$P_{off} = E_T * f$$

Hence the total power, P_T, dissipated in an integrated switch with multiple output sections is:

$$P_{T(av)} = (P_{off} + P_{on}) * n + P_{(quies)}$$

This is the average power dissipation for multiple sections whose duty cycles have a fixed time relationship to each other. For multiple outputs with variable duty cycles the power calculation becomes more difficult.

Where,

E_T	=	Total turn-off transient energy absorbed
f	=	Switching frequency
d	=	Duty cycle
L	=	Load Inductance
I_P	=	Peak output load current
n	=	Number of output switches operating
P_{off}	=	Turn-off power dissipation in each switch
P_o	=	On-state power dissipation each switch
$P_{(quies)}$	=	Interface device bias power dissipation
$P_{T(av.)}$	=	Average total power dissipation
R_L	=	Resistance of inductor
V_{CL}	=	Clamp voltage
V_{SS}	=	Load supply voltage

2.4 Thermal Considerations

With the device total power dissipation calculated now a thermal evaluation can proceed. The objective is to determine if external heat sinking will be required.

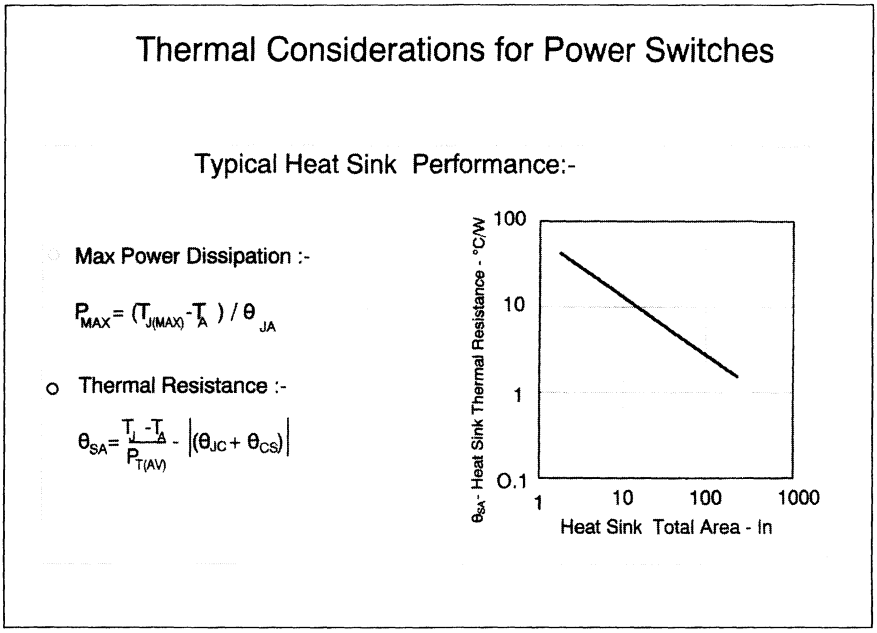


Figure 4.2.5 Thermal Considerations For Power Switches

The requirement for external heat sinking is calculated based on the device's total average power dissipation, maximum junction temperature, and ambient operating temperature. The maximum power which can be dissipated in a device (P_D) can be determined as follows:

$$P_D = (T_J - T_A) / (R_{\theta JA})$$

Where: T_J = Maximum device junction operating temp.

T_A = Maximum ambient operating temp.

$R_{\theta JA} = \theta_{JA}$ = Junction to ambient thermal resistance, °C/W

T_J and $R_{\theta JA}$ are taken from the device specification and TA is determined by the application environment.

Is a heat sink required?

If the total power dissipated in the device P_T exceeds the maximum power dissipation P_D then either a heat sink must be used or a different device must be selected.

A heat sink size can be determined by first calculating the required heat sink to ambient thermal resistance $R_{\theta SA}$ as follows:

$$R_{\theta SA} = [(T_J - T_A)/P_{T(AV)}] - [R_{\theta JC} + R_{\theta CS}] \qquad (\theta_{SA})$$

Where:

$R_{\theta JC}$ = device junction to case thermal resistance (θ_{JC})

$R_{\theta CS}$ = case to heat sink thermal resistance, °C/W (θ_{CS})

= 0.5 /W typical with thermal joint compound

$P_{T(AV)}$ = total average power dissipation, W

T_J = junction operating temperature, °C (from data sheet)

T_A = operating ambient temperature, °C

The $R_{\theta SA}$ required can now be compared to heat sink design specifications to determine the design type and size required.

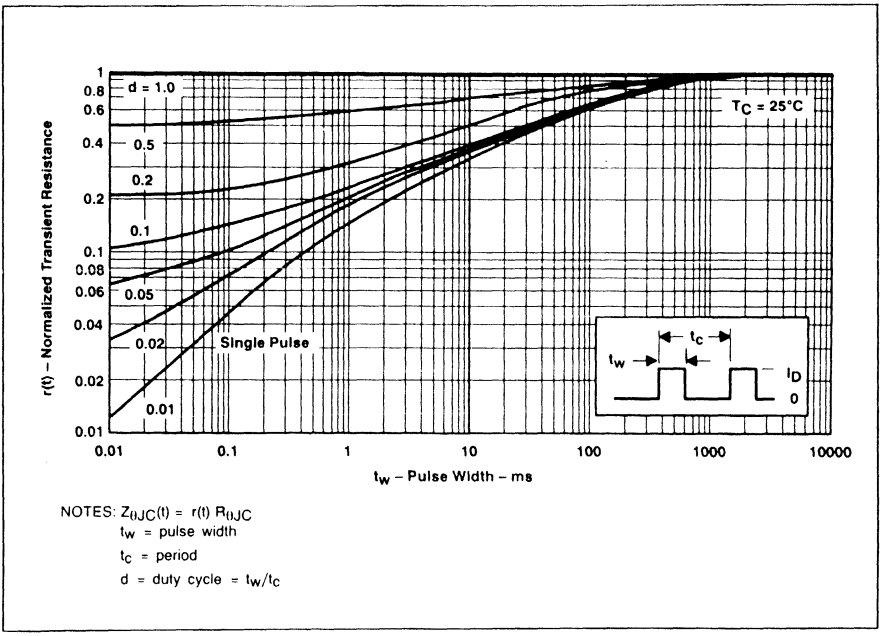


Figure 4.2.6 Power+ Arrays Thermal Impedance Characteristics

The preceding thermal calculations were based on the assumption that the device average power was duty cycle dependent. This is true if the pulse widths are short in relation to the device thermal time constant. An example would be a switch that is "on" for one hour in every twenty four hours. The actual duty cycle is low but your system must be designed to accommodate 100% on time for the switch. The graph in Figure 4.2.6 gives the times associated with the TO-220 Power+ Arrays.

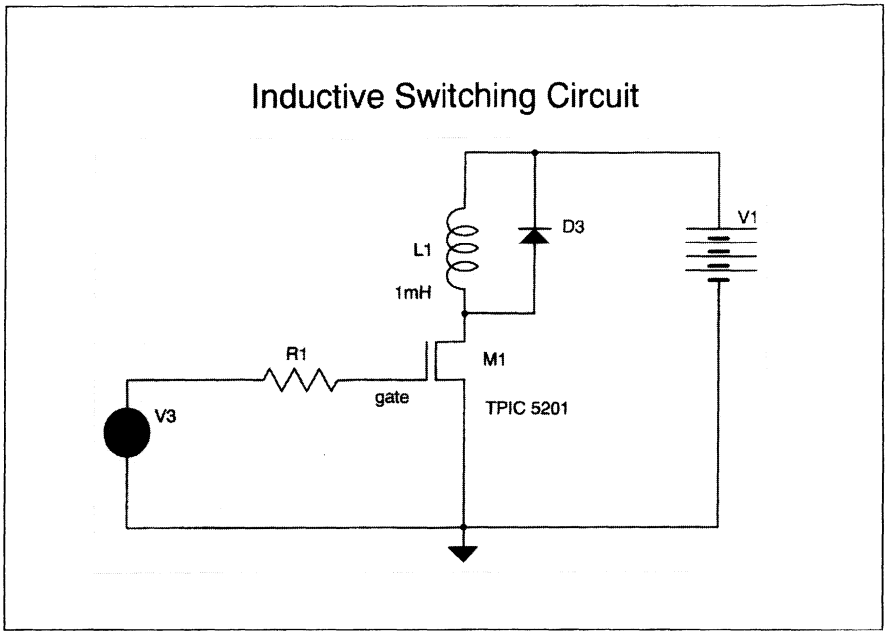


Figure 4.2.7 Inductive switching circuit

2.5 Switching Speed

The delay and transition times that occur during the switching transients of the device can easily be determined with the aid of characterisation data given within the data sheet. Consider the simplified circuit diagram and associated waveforms shown in figures 4.2.7 and 4.2.8 in which is shown a typical inductive load whose recirculation current is being controlled by transistor M1.

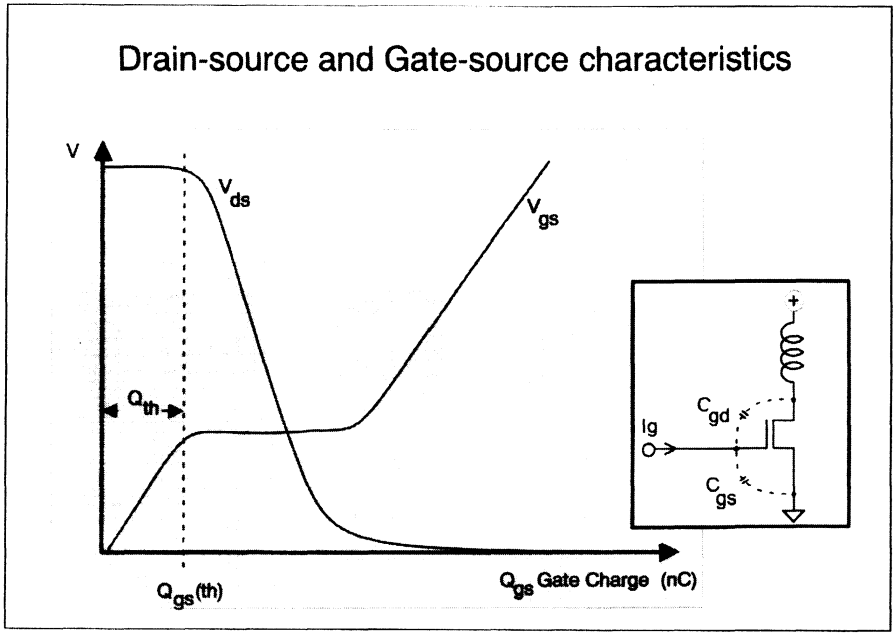


Figure 4.2.8 Associated gate-source and gate-drain waveforms

In Figure 4.2.8, a useful mnemonic for the gate charge/time relationship is that a nano-Coulomb (nC) of charge is equivalent to 1 μs. Thus the horizontal axis may be read directly in microseconds of delay, if the charging current is a constant 1 mA, or scaled to the current available.

The drain current of the mosfet is controlled by the gate source voltage. This relationship is shown in figure 8 of the TPIC5201 data sheet, and is elaborated below in figures 4.2.9 and 4.2.10.

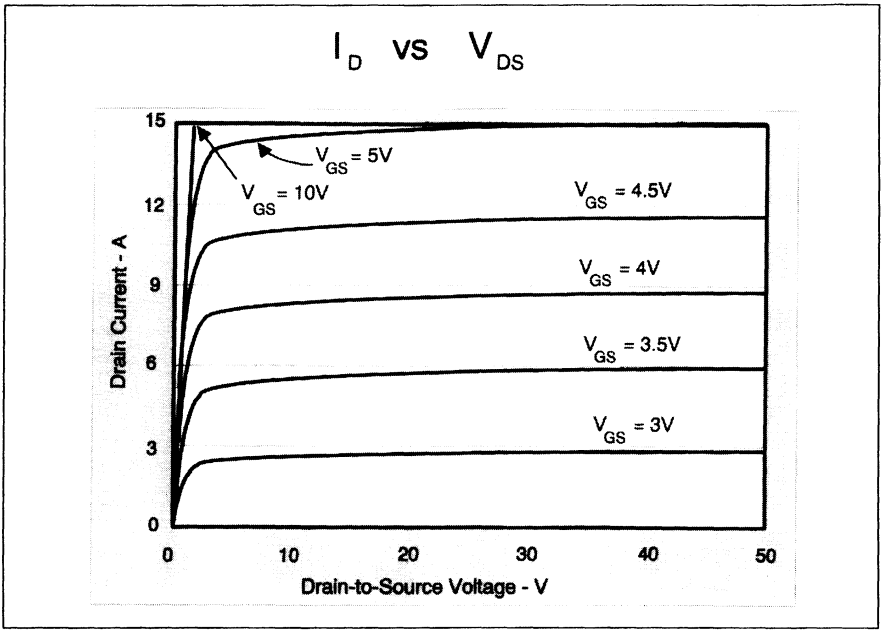


Figure 4.2.9 TPIC5201 transfer characteristics

Careful study of figure 4.2.10 indicates three distinct regions of operation. Firstly, at low gate voltages, below the threshold voltage, V_{th}, the mosfet is in the off-state and no drain current flows. The threshold voltage is specified in the data sheet at 1mA as typically 1.75V. Above the threshold voltage the drain current is linearly related to the gate voltage by:

$$I_d = g_{fs}(V_{gs} - V_{th}) \quad \text{.....(1)}$$

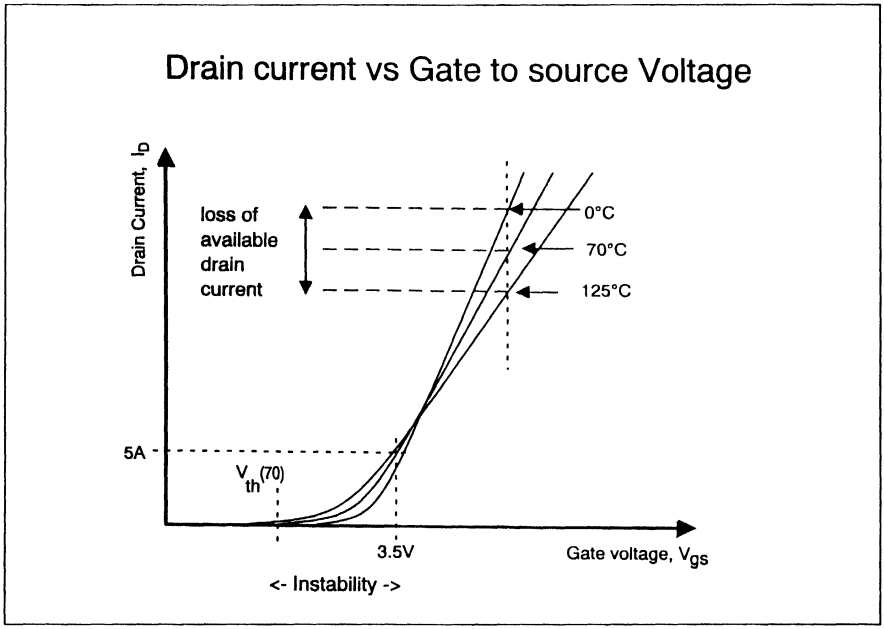


Figure 4.2.10 Effect of Temperature on transfer characteristics

The data sheet specifies the magnitude of g_{fs} at 5A as typically 4.7 Siemens. The second region in figure 4.2.10 occurs between the threshold voltage and the point where the drain current exhibits a positive temperature coefficient with respect to the gate voltage. The third region occurs at gate voltages greater than this, where a negative temperature relationship exits between drain current and gate voltage.

Essentially, the dynamic input characteristics of the power mosfet may be regarded as capacitive, however, due to the physical construction of the device the terminal capacitances are a function of the applied voltage. Consequently, the dynamic relationship between actual gate voltage and the applied drive signal are best described by the use of charge transfer.

In figure 4.2.11 overleaf is the gate charge waveform of a typical array device. In this figure, three regions may also be distinguished.

The first region is described by Qgs(th) and represents the charge required to raise the gate-source capacitance voltage to that necessary for control of the drain current. Fig 11 on the data sheet suggests a Qgs(th) at a drain current of 2.5A of typically 1.5nC.

The V_{gs} required to maintain a drain current of 5A may be obtained with the aid of the data sheet or figure 4.2.9 or 4.2.10 above as nominally 3.5V. An input capacitance may be associated with this region of low gate-source voltage, V_{gs} and is calculated as follows:

since, $$Q = CV \quad \text{.....(2)}$$

$$C_{in} = \frac{Q}{V} = \frac{1.5nC}{3.5V} \quad \text{.....(3)}$$

$$= 430 \text{ pF}$$

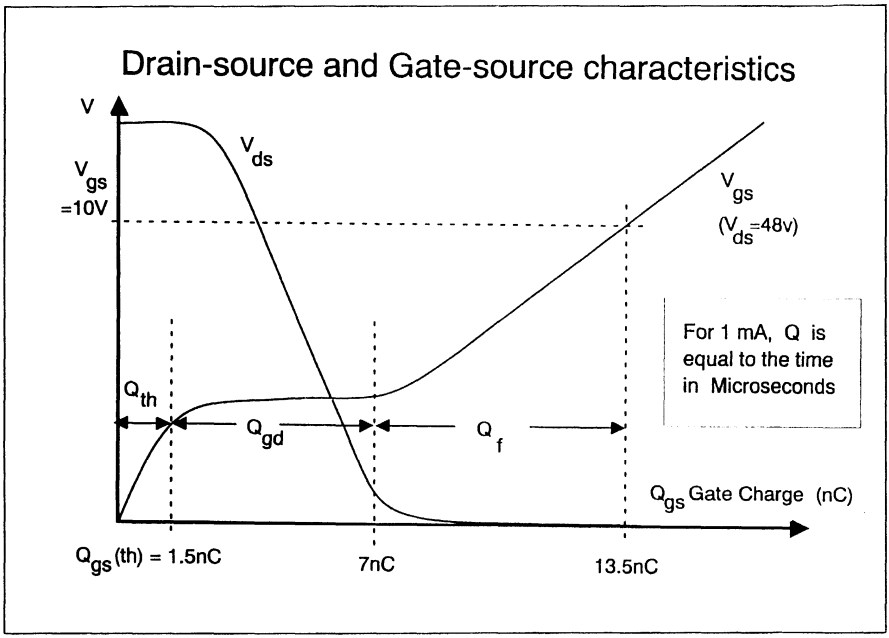


Figure 4.2.11 gate charge waveforms

The second region, referred to as Qgd in figure 4.2.11 above, is the charge required to fully charge the gate drain capacitance, which is a function of the source-drain voltage.

Assuming the device is switching from a 48 volt rail, the magnitude of this charge is may be obtain from figure 4.2.11 above as:

$$7nC - 1.5nC = 5.5 \text{ nC}$$

The third region given by: $Q_g - Q_{gd} - Q_{gs(th)}$ is the charge required to charge the input capacitance to the input drive voltage, and has no impact on the actual drain current. The difference between the initial and final slope of the V_{gs} vs. Q_g curve may be attributed to the difference in value of the drain-gate capacitance.

From a drive circuit perspective, it should be noted that the effective input capacitance, C_{in} does not have the same magnitude when the device is being turned on as when

turned off. At turn on, the drain source voltage will be high, and a C_{rss} value at high V_{ds} and C_{gs} value at low V_{gs} would be appropriate, and at turn off capacitance values at low V_{ds} and high V_{gs} would apply.

The value of the appropriate input capacitance may also be obtained from the slope of the gate charge curve for high and low values of V_{gs}.

2.6 Calculation of Switching speeds

2.6.1 Turn-on

The rise and fall times of the drain during switching may be limited by a number of factors relating to both the gate and drain circuits. It is assumed in the following analysis that the drain inductance and capacitance have a time constant that does not limit the drain slew rate and that the response of the device is controlled by the gate drive circuit.

The gate resistance seen by the device, R_g, is the sum of the intrinsic gate resistance and that of the drive circuit; 0.25 ohms is a typical value for gate input resistance. When the drive signal is initially applied, the gate capacitance, C_{in}, charges through the input resistance until the threshold voltage occurs: at this point, the drain starts to conduct current, and the input capacitance continues to charge to a voltage level that will sustain the drain current. The time taken for the gate RC network to reach the threshold voltage gives rise to a delay time, t_{delay}, which is given by:

$$t_{delay} = C_{in} R_g \ln\left(1 - \frac{V_{th}}{V_{gg}}\right)^{-1} \quad \text{.....(4)}$$

where V_{gg} is the magnitude of the drive signal.

The gate voltage required to support the drain current is obtained from the transfer characteristics of equation (1) as:

$$V_{gs(active)} = \frac{I_d}{g_{fs}} + V_{th} \quad \text{.....(5)}$$

Therefore, given a supply voltage ,V_{gg}, the rise time of the current to reach a value I_d is given by the time required for the input $R_g C_{in}$ network to charge from an initial voltage of V_{th} to $V_{gs(active)}$. During this period, the drain current is given by:

$$I_d = g_{fs}\left\{ V_{gg}\left(1 - \exp\left(\frac{-t}{C_{in} R_g}\right)\right) - V_{th} \right\} \quad \text{.....(6)}$$

The sum of the rise time and delay time may be obtained from the equation(6) above by setting I_d equal to the load current, I_l, being switched.

$$\therefore t_{ri} + t_{dom} = R_g C_{in} \ln\left(\frac{V_{gg} g_{fs}}{V_{gg} g_{fs} - I_l - V_{th} g_{fs}}\right) \quad \text{.....(6a)}$$

Once the load current is established in the device, the drain voltage is free to fall from the supply voltage to its on-state voltage. In doing so, the gate-drain capacitance, C_{gd} must be charged; this charge will be supplied from the gate drive circuit. Since the drain current does not vary during this period, the gate-source voltage will be constant and the input gate current is given by:

$$I_g = \left(\frac{V_{gg} - V_{gs(active)}}{R_g}\right) \quad \text{.....(7)}$$

Where the magnitude of $V_{gs(active)}$ is given by equation (5)

The rate of change of drain voltage is given by:

$$\frac{dv_{gd}}{dt} = \frac{I_g}{C_{gd}} \quad \text{.....(8)}$$

Therefore, given a load supply V_{dd}, the fall time is given by:

$$t_{fv} = \frac{V_{dd} C_{gd}}{I_g} \quad \text{.....(9)}$$

In practice, equation 9 is difficult to apply since the magnitude of C_{gd} is a strong function of gate-drain voltage. At low voltages the magnitude of C_{rss} (C_{rss}=C_{gd}) tends to increase significantly. Further, the magnitude of C_{rss} increases above this value for negative values of gate-drain voltage, which occur when the device is fully switched on. An alternative approach to calculating the fall time is possible by associating the plateau region of the gate charge curve with the charge necessary to fully charge the gate-drain capacitance.

The gate charge curves show that the total needed to fully charge the gate-drain capacitance is approximately 7nC (V_{ds}=48V), and therefore the charge required by the gate-drain capacitance is given by:

$$GateCharge = 7nC - Q_{gs(th)} \quad \text{.....(10)}$$

$$\therefore t_{fv} = \left(\frac{5.5nC}{I_g} \right) \quad \text{.....(11)}$$

where I_g is given by equation 7 above.

2.6.2 Turn-off

During turn-off the gate source capacitance is discharged through the gate resistance R_g. However, due to the asymmetry of the gate charge curve, the turn-off and turn-on periods will be different.

It should be noted that the input capacitance, C_{in} does not have the same value as in the case of turn-on, since the gate-drain capacitance increases in magnitude as the source-drain voltage is reduced. The value of the appropriate capacitance may be obtained from the slope of the gate charge curve for high values of V_{gs}.

Initially, the gate capacitance discharges from the supply, V_{gg}, to $V_{gs(active)}$. Thus, by combining the RC discharge rate with the gate transfer function, the delay time is obtained:

$$V_{gs} = V_{gg} \exp\left(\frac{-t}{R_g C_{in}} \right) \quad \text{.....(12).}$$

$$t_{d(off)} = R_g C_{in} \left(\frac{V_{gg}}{V_{th} + \frac{I_l}{g_{fs}}} \right) \quad \text{.....(13)}$$

Once the gate voltage has fallen to $V_{gs(active)}$, the drain voltage is free to rise towards the supply voltage. As in the turn-on case, the gate-drain capacitance, C_{dg}, must be charged, and the voltage rise time is given by:

$$t_{rv} = \frac{C_{gd} V_{dd}}{I_g} \quad \text{.....(14)}$$

As previously noted, the plateau region of the gate charge curve is associated with the rise in drain voltage and may be used to derive an equation similar to equation (11).

When the drain voltage reaches the supply rail, the clamping diode is free to turn on and the gate voltage will discharge through the gate resistance and be given by:

$$V_{gs} = \left(V_{th} + \frac{I_l}{g_{fs}} \right) \exp\left(\frac{-t}{R_g C_{in}} \right) \quad \text{.....(15)}$$

Equation (15) may be used in conjunction with equation (1) to give the resulting drain current:

$$I_d = \left(I_l + g_{fs} V_{th} \right) \exp\left(\frac{-t}{R_g C_{in}} \right) - g_{fs} V_{th} \quad \text{.....(16)}$$

The fall time is obtained by setting I_d=0 or by using the discharge rate of the gate resistance/capacitance combination, i.e.

$$t_{fi} = R_g C_{in} \ln\left(1 + \frac{I_l}{g_{fs} V_{th}} \right) \quad \text{.....(17)}$$

2.7 Worked example:

Consider the case of switching the TPIC5201 with the following parameters:

R_g = 100, V_{gg} = 10, L = 10mH, I_l = 5A and V_{dd} = 48V.

The data sheet may be used to obtain the following:

1/ From the transfer curves, $V_{gs(active)}$ = 3.5V

2/ $Q_{gs(th)} = 1.5$ nC

3/ $V_{th} = 1.75$ V

4/ $g_{fs} = 4.7$ S

The input capacitance for low V_{gs} values is

$C_{in} = 1.5nC/3.5V = 430pF$

The input capacitance for high Vgs is

$$C_{in} = \frac{Q_{gs}(10V) - Q_{gs}(3.5)}{10 - 3.5} = \frac{13.5 - 7}{10 - 3.5} = 1000 \text{ pF}$$

2.7.1 Switch-on

The delay time, t_{don} is given by application of equation (4) :

$$t_{don} = C_{in} R_g \ln\left(1 - \frac{V_{th}}{V_{gg}}\right)^{-1}$$

$$t_{don} = 430 \times 10^{-12} \times 100 \times \ln\left(1 - \frac{1.75}{10}\right)^{-1}$$

$$= 8.3\text{ns}$$

Equation (6) is used to obtain the rise time as follows:

$$t_{ri} + t_{don} = R_g C_{in} \ln\left(\frac{V_{gg} g_{fs}}{V_{gg} g_{fs} - I_l - V_{th} g_{fs}}\right)$$

$$t_{ri} + t_{don} = R_g C_{in} \ln\left(\frac{10 * 4.7}{10 * 4.7 - 5 - 1.75 * 4.7}\right)$$

$$\therefore t_{ri} = 100 \times 430 \times 10^{-12} \times 0.33 - 8.3ns$$

$$= 5.9 \text{ ns}$$

The voltage fall time is calculated by first calculating the gate current and using the charge transfer curve:

$$I_g = \frac{V_{gg} - V_{gs(active)}}{R_g}$$

$$I_g = \left(\frac{10 - 3.5}{100}\right) = 65mA$$

$$t_{rv} = \frac{7nC - 1.5nC}{65mA} = 84ns$$

2.7.2 Switch-off

The delay time is obtained from equation (13):

$$t_{doff} = R_g C_{in}\left(\frac{V_{gg}}{V_{th} + \frac{I_L}{g_{fs}}}\right)$$

$$t_{doff} = 100 \times 1000pF \times \frac{10}{1.75 + \frac{5}{4.7}}$$

$$t_{doff} = 355ns$$

the voltage rise time, t_{rv} is given by:

$$t_{rv} = \Delta Q_{gs} / I_g = (7nC - 1.5nC) / 35mA = 157ns$$

$$\text{(where } Ig = \frac{0 - V_{gs(active)}}{R_g} = \frac{-3.5}{100} = \text{-35 mA)}$$

and the fall time is given by equation (17) as:

$$t_{fi} = R_g C_{in} \ln\left(1 + \frac{I_l}{g_{fs} V_{th}}\right) = 100 * 430pF * \ln\left(1 + \frac{5}{4.7 * 1.75}\right)$$

= 20 ns

2.8 Conclusion

Defining the system output requirements leads to selection of a load, based on load output specifications.

From the load characteristics, system energy can then be calculated, and the load input specifications derived along with some switch assumptions.

A switch device can then be selected on peak and average power and energy calculations. Load analysis will then indicate whether external circuitry for back e.m.f. energy dissipation is needed.

For array devices, examination of the data sheet charge characteristic and gate drive available will give an estimate of the switching time of the output.

A thermal analysis based on the selected device thermal specifications will determine if additional heat sinking will be required.

The design of the switch section will be completed when actual measurements from the system are used to verify the design. These measurements must include dynamic measurements using an oscilloscope or similar method to view the current and voltage waveforms, verifying that they agree with the design assumptions.

This is the single most critical element of the design flow - testing and evaluating the prototype, and if in doubt, redesigning to add greater margins of safety, and then re-testing to confirm.

3 Applications - Stepper Motors

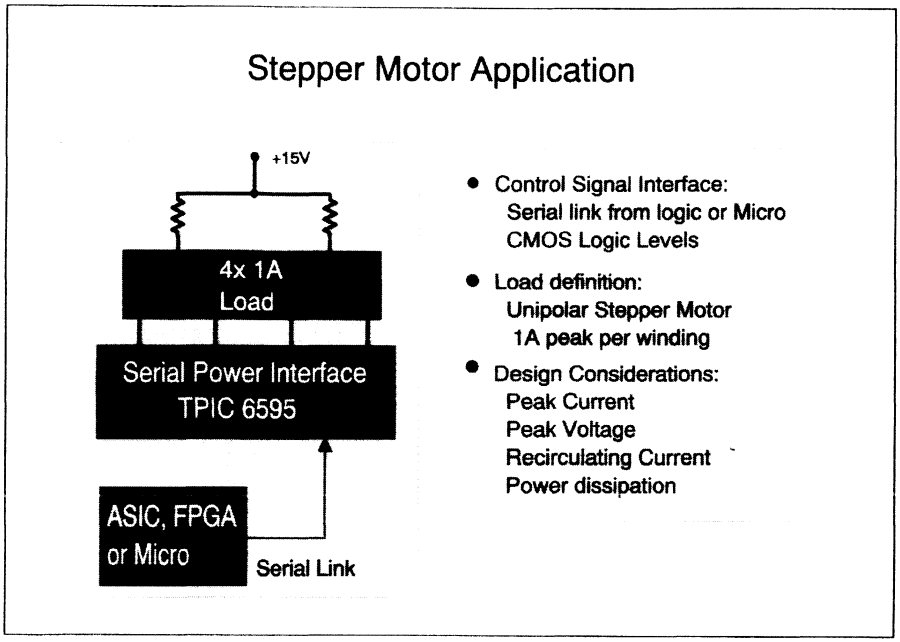


Figure 4.3.1 1-Amp Stepper Motor Application

3.1 1-A Stepper Motor Application with serial interface

Stepper motors are often chosen to provide incremental rotating motion. Some typical applications are printers, copiers, and industrial robots. They are increasingly found in automotive systems, as more in-car functions are automated. Stepper motors present a multiple phase inductive load to the output circuit.

Figure 4.3.1 shows a block diagram of the application. The motor chosen has unipolar windings which require a peak current of 1A.

3.1.1 Load Description:

The first consideration in designing this application is to consider the load which in this case is a one amp unipolar stepper motor. The permanent magnet rotor stepping motor has two forms of stator winding. The bipolar stepping motor has a single winding on each stator pole and uses a full bridge to drive each phase winding. In the unipolar stepping motor, the flux reversal is accomplished by individually driving a bifilar winding on each pole.

The windings are phased such that when current is passed through one winding, a given flux direction is generated. By passing current through the other winding, the opposite flux polarity is produced. Thus, the overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by interface devices with open-drain outputs.

The motor chosen for this application has unipolar windings. Due to the manner in which the windings are constructed, a back e.m.f. voltage will be induced both in a winding that was turned off and in the other bifilar winding.

3.1.2 Energy Calculations

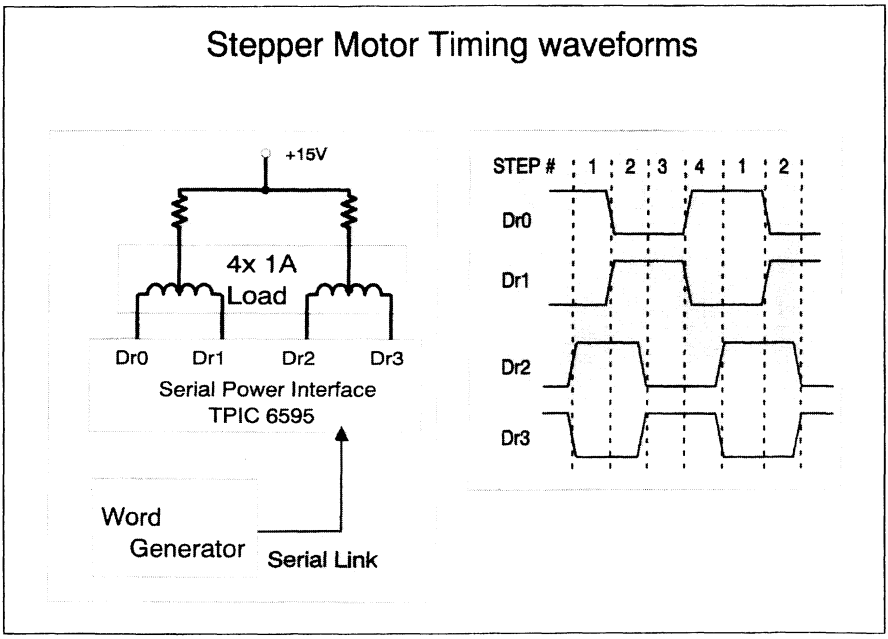


Figure 4.3.2 Stepper Motor Timing Waveforms

Figure 4.3.2 shows a timing waveform of the stepping motor. The table in the lower right section shows the winding switching sequence. Additionally we can see that at any step two windings will be energized. With the knowledge that the windings are driven two at a time and by observation of the current waveform we can begin energy calculations. The value of back e.m.f. energy will remain the same as if it were all returned to one winding.

Observation of the timing diagram indicates t_{on} = 5 ms and that the winding current approximates a linear ramp (L/R >> t_{on}). This indicates that the simplified formula will be a good approximation.

Therefore:

$$P_{on} = 1/3\ (I_P{}^2)*R_{DS(on)}*d$$

Where d = 0.5 (each winding conducts twice in the four step cycle)

Note that in this example if the motor is stopped the current through each winding will be a steady 1 A. This brings up an important point. The power calculations are based on an assumed operating frequency. If the motor is stopped the individual drive currents may exceed the maximum continuous current rating of the switches. When calculating energy and power, worst-case assumptions must be considered.

3.1.3 Choosing an Interface Circuit

Figure 4.3.2 shows a TPIC6595 that has been chosen for this application because it can meet the power requirements, can drive all four 1 Amp windings from a single integrated circuit, and includes interface logic.

The same figure also shows the TPIC6595 driving the stepper motor at its rated 1 amp by operating two output DMOS transistors in parallel. Drain 0 (Dr 0) is representative of output transistors 1 and 5 in parallel. Similarly, Dr 1 is representative of output transistors 2 and 6, etc. Anti-parallel source-drain diodes are omitted for clarity.

In this example, the input data which would normally be provided by the system's microprocessor, random logic, FPGA etc. was provided by a Hewlett Packard HP8180A data generator.

The antiparallel diodes are used to recirculate the current that is induced in the winding when the current through the previously activated winding on the pole is terminated. Hence, during each motor revolution both positive and negative current flows through the power switches which control the winding. Fig 4.3.3 illustrates the voltage and current flows for Drain 0.

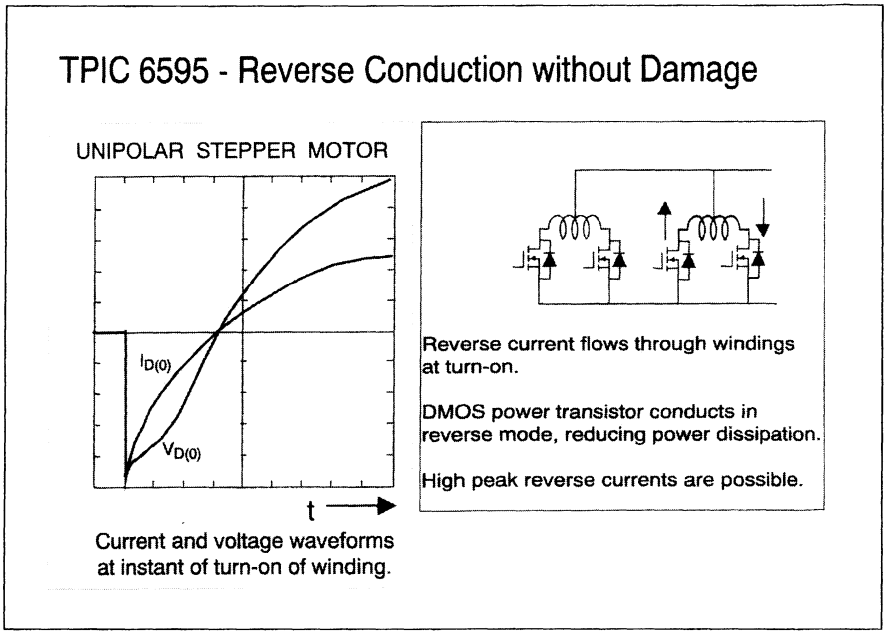


Figure 4.3.3 TPIC6595 Stepper motor turn-on waveforms

Two features of the Power+ Logic DMOS output structure enhance the performance of the outputs when switching inductive loads as in the previous stepper motor example. Figure 4.3.3 shows an expansion of the wave forms of the negative current region of the winding pulse from the stepper motor application.

As previously mentioned, the anti-parallel diodes of the DMOS output allow the recirculation of current at winding turn-on. It is the anti-parallel diode which allows the DMOS output to withstand high peak reverse currents. In contrast, a power bipolar structure does not benefit from an inherent anti-parallel diode; one must be physically added, either to the integrated circuit design, or externally at the board level.

If negative currents are required of a bipolar power switch which does not include such as diode, parasitic isolation diodes in the bipolar structure will conduct which may cause system malfunction. It is for this reason that a DMOS solution is often the most practical and economical for motor drive applications.

Returning to the stepper motor example, as the winding turns on, the voltage drop across the output decreases. Once the voltage drop across the output ceases to be at least 0.7V, the body drain diode no longer conducts. At this point, the DMOS power transistor turns on in the reverse direction, allowing continued negative current flow to the inductor.

Once reverse conduction through the DMOS becomes the vehicle for negative current flow to the inductor, the power dissipation is given by the product of $R_{DS(on)}$ and the square of the drain current. Reverse conduction continues through the DMOS transistor until the current reaches zero.

Why choose a Power+ Logic device for an application:

- The DMOS output structure is power efficient, reducing system dissipation and heat-sinking
- TPIC6Axxx parts have current limited output protection
- The output structure is fully specified to withstand high avalanche energy.
- System design is simpler than with discrete DMOS or bipolar transistors.
- The PCB layout is substantially more compact due to the integration of power and logic, and the lack of external protection passives in most systems.

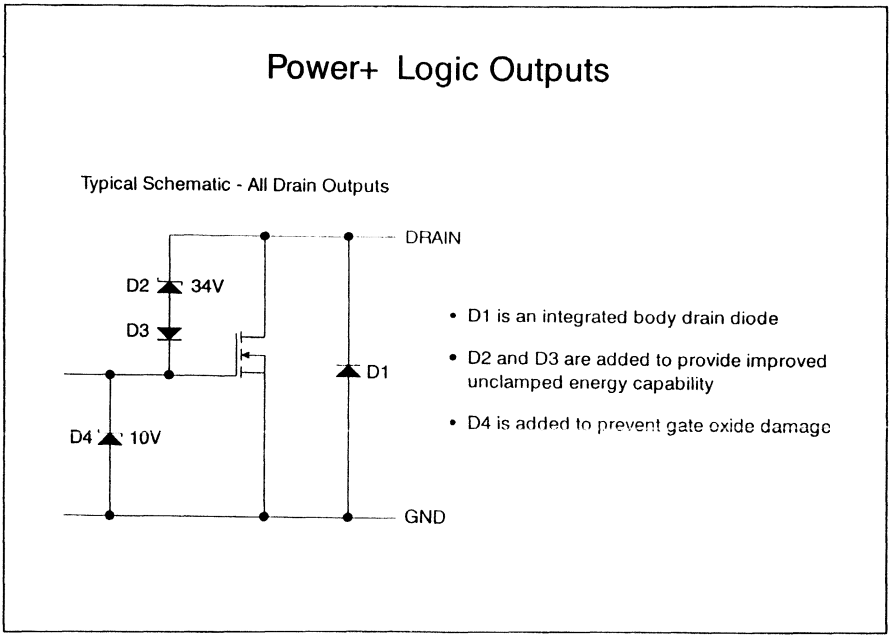


Figure 4.3.4 Power+ Logic Output Structure

The TPIC6595 device has 8 power DMOS outputs with built-in 45V voltage clamps for enhanced inductive energy switching capability. When switching inductive loads, high voltage transients are seen at the device output when the output is placed in a high impedance state. The voltage generated by the inductive transient is limited by the breakdown mechanism of the output structure.

For the TPIC6xxx Power+ Logic devices, the internal dynamic 45V clamp circuit will eventually conduct during switching of an unclamped inductive load, allowing current to charge up the gate of the DMOS.

Once the DMOS gate voltage exceeds the threshold voltage of the device, the DMOS turns back on, completely dissipating the energy from the inductor. Thus, the entire active area of the DMOS transistor is used in the forward bias mode to absorb energy from the inductive load.

Without the internal clamp circuitry, the device output would be driven into avalanche breakdown, and would operate in the much lower energy capability reverse bias mode. The built-in voltage clamps of the Power+ Logic devices allow the user to switch up to 75 mJ of avalanche energy without the use of external snubber circuitry.

Each DMOS output of the TPIC6595 can provide 250 mA of continuous current with all outputs turned on. Individually, the outputs can be pulsed to provide up to 1.5 A of current. Or, multiple outputs can be parallelled for increased current drive of up to 6A of pulsed total load current. This rating is sufficient to drive the stepper motor when operating at the described duty cycle.

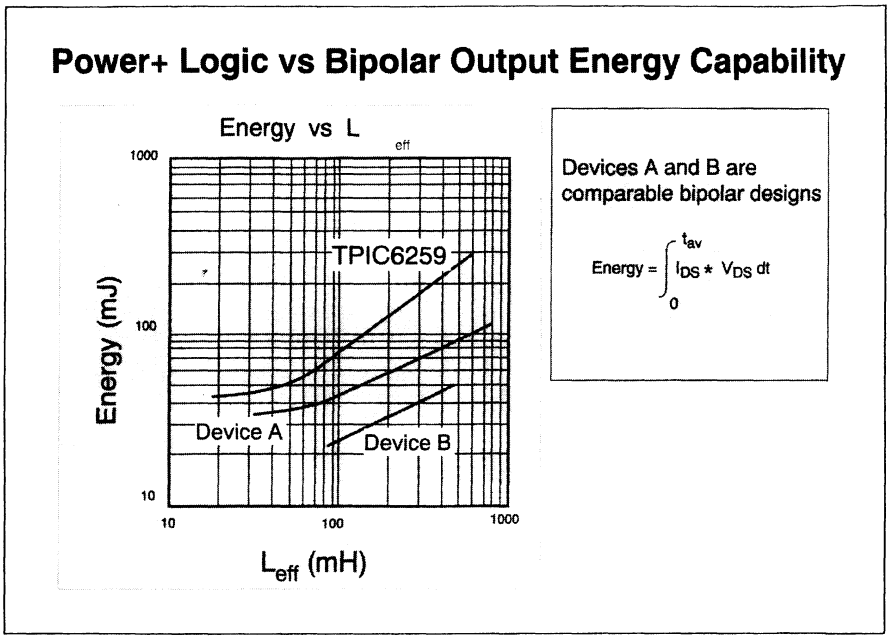


Figure 4.3.5 Power Logic Vs Bipolar Output Energy

In describing the ruggedness of any power output, a key parameter is the avalanche energy capability. When the maximum energy capability is determined by thermal limitations of the silicon, the energy that can be dissipated during avalanche is not a constant, but varies with peak switching current and load inductance. Some power structures, however, may be prematurely limited by secondary breakdown and will have a constant energy rating. For an inductive switching pulse within the energy capability of the device, the energy dissipated in the output is proportional to the product of the current and voltage waveforms.

Figure 4.3.5 benchmarks the ruggedness of the Power+ Logic devices against two low side bipolar devices having comparable voltage capability. Device A has a breakdown voltage of 37V, while device B has a breakdown voltage of 50V. Each bipolar device has approximately twice the output active area as the Power+ Logic devices. The data in the figure reflects the last point of output survival just prior to its destruction.

It is evident that the Power+ Logic DMOS device is much more rugged that either of the bipolar structures. While switching a 350 mH inductor, the TPIC6259 dissipates 200 mJ prior to destruction, more than twice the energy of the bipolar devices. Note that while the energy capability of the Power+ Logic devices decrease to 45 mJ while switching a 30mH load, this is still significantly more than comparable bipolar devices. This implies substantially improved safety margins when using Power+ Logic solutions.

Unclamped Inductive Switching Test Data

Maximum Energy Capability Prior to Device Destruction
T_j = Starting Junction Temperature = 25 °C

Device Type	I_{AS} (A)	t_{av} (ms)	V (V)	V (V)	L_{eff} (mH)	L (mH)	E (mj)	P_O (W)	K	T_m Deg C	T_{jpk} **Deg C**
DMOS	2.1	0.8	50	15.1	19	13.2	42.2	105.5	269.0	378	**403**
TPIC6259	1.7	1.4	50	15.1	42	29.4	58.1	83	269.0	394	**419**
Bipolar	1.3	1.5	37	9.0	41	30.7	35.4	48.8	139.5	122	**147**
Device A	0.9	2.6	37	12.8	101	66.3	43.9	34.4	139.5	114	**139**
	0.8	5.0	37	19.0	247	120.0	69.4	27.8	139.5	129	**154**
Bipolar	0.8	1.3	50	11.6	80	61.4	25.6	40.0	139.5	94	**119**
Device B	0.7	1.8	50	9.5	125	101.0	30.6	35.0	139.5	96	**121**
	0.5	3.4	50	15.0	335	335.0	41.9	25.0	139.5	95	**120**

$$\text{Energy} = \int_0^{t_{av}} I_{DS} * V_{DS}\, dt$$

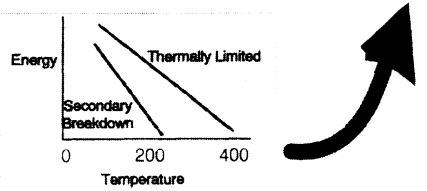


Figure 4.3.6 Unclamped Inductive Switching Test Data

In addition to peak switching current and load inductance, the energy capability of a power device varies with temperature. As the junction temperature of the device increases, energy capability decreases. This temperature-energy relationship was exploited to further understand the avalanche energy capabilities of the Power+ Logic devices.

Unclamped inductive switching tests were performed on the Power+ Logic devices in which the junction temperature of the DMOS output was gradually raised by forcing the device to dissipate increasingly large amounts of energy. The virtual junction temperature of the device immediately prior to destruction was calculated.

Note that for the purposes of these tests, the 150°C maximum junction temperature specification of the Power+ Logic devices was violated; these tests do **not** reflect recommended operation of the Power+ Logic devices.

Assuming mechanical limitations of the package are disregarded, the maximum avalanche energy capability of a power device operating in the forward bias mode is limited by the thermal capabilities of silicon. However, the actual avalanche energy

dissipated by a given power structure may be prematurely limited by a secondary breakdown mechanism.

In the case of the Power+ Logic outputs, the absence of forward secondary breakdown can be shown. The calculated virtual junction temperature of the Power+ Logic output structure at the point of device destruction was greater than 400°C. Since silicon is thermally limited at approximately 400°C, silicon thermal limitations were the probable cause of device destruction.

For comparison, similar tests were performed on the bipolar devices A and B. Bipolar device B (50V clamp) had a calculated maximum virtual temperature of approximately 120°C immediately prior to destruction, clearly illustrating a secondary breakdown limitation. Bipolar device A (37V clamp) had improved characteristics, but still clearly experienced secondary breakdown limitations with destruction temperatures ranging from approximately 140°C to 150°C.

The following terms and definitions apply to figure 4.3.6:

I_{as} = Peak current reached during device avalanche

t_{av} = Time duration of device in avalanche

L = Load inductance

L_{eff} = Effective load inductance; accounts for supply voltage

E = Energy absorbed by device under test $L_{eff} \times I_{as}^2/2$

V_{dd} = Output supply voltage

V_{dsx} = Effective device avalanche voltage

T_c = Case temperature

T_M = Maximum junction rise which occurs in inductive switching

P_o = Power = $I_{as} \times V_{dsx}$

K = 139.5 = A thermal constant where the area of active silicon = 1k mils square.

K = $2/(A(p\ kc)^{1/2})$ where A = Area of power gen. silicon
p = density of silicon
k = thermal conductivity of silicon
c = thermal capacity of silicon

T_M = $(2^{0.5})/3\ Po\ k(tav)^{0.5}$

T_{JPK} = Peak junction temperature at point of destruction = $T_M + T_c$

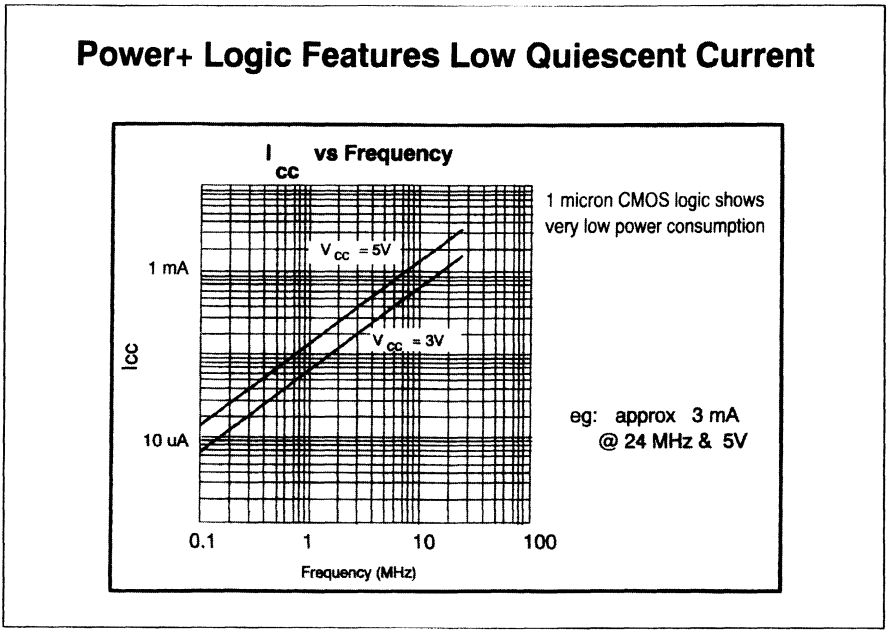


Figure 4.3.7 Power+ Logic Features Low Quiescent Current

The Power+ Logic devices integrate performance power output structures with high-density sub micron CMOS logic. Figure 4.3.7 shows Icc versus SRCK frequency for the TPIC6595 with the outputs static and an alternating bit pattern on the SER IN pin. This example demonstrates the high logic frequency capability of the Power+ Logic devices, as well as the low Vcc power consumption. A high logic speed capability allows the information to be transferred from the µP, FPGA or ASIC interface very quickly even though the switch and load operation occurs at a much slower repetition rate. This would especially be important when cascading several devices for a large number of outputs all controlled by a single serial interface, as in LED (or incandescent lamp) video arrays.

The power described in this graph is the term P_{quies} used in calculating the total average power dissipated in a device.

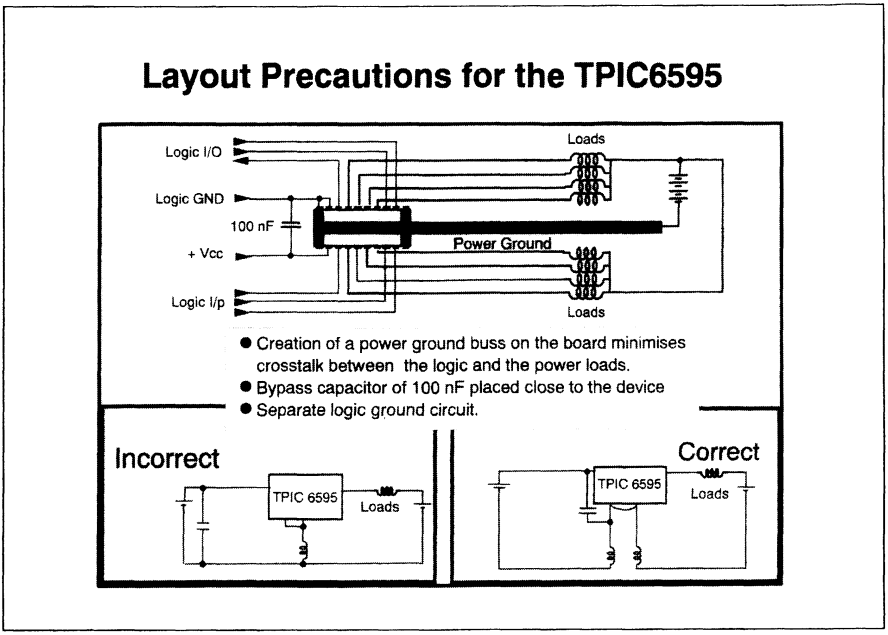


Figure 4.3.8 Layout Precautions for the TPIC6595

When using the TPIC6595, or any of the Power+ Logic devices, there are several PCB layout considerations which should be kept in mind. High frequency layout rules should be used when designing any power switching systems as mutual inductance (i.e. coupling between the drive circuit and load circuit) can cause erroneous signals which result in false operation. In figure 4.3.8, the "Incorrect" sketch shows an undecoupled mutual inductance in the power and logic ground. This is not a separate inductor - it represents the inductance of the common ground trace, to illustrate the nature of the problem. The following precautions are offered:

- Use of a heavy duty power ground buss on the PCB to eliminate crosstalk between the power loads and input logic.
- Addition of a 0.1 µF bypass capacitor between V_{cc} and the logic ground line, placed close to the device to dampen any stray signals experienced by the drive circuit.
- Separate power and logic ground circuits.

Figure 4.3.8 shows an example implementation of these board layout considerations using the TPIC6595.

3.2 Stepper Motor Applications made easy with TPIC2404

The TPIC2404 is a monolithic quad intelligent-power 45V, 1 Amp low-side switch in a small 15-pin zig-zag in-line power package. Its switching efficiency means most applications avoid a heat sink, saving power and board space. Comprehensive error circuitry detects overvoltage, open load (or short to ground), short to Vcc and thermal sensing. This shuts down the power devices and produces a FAULT output.

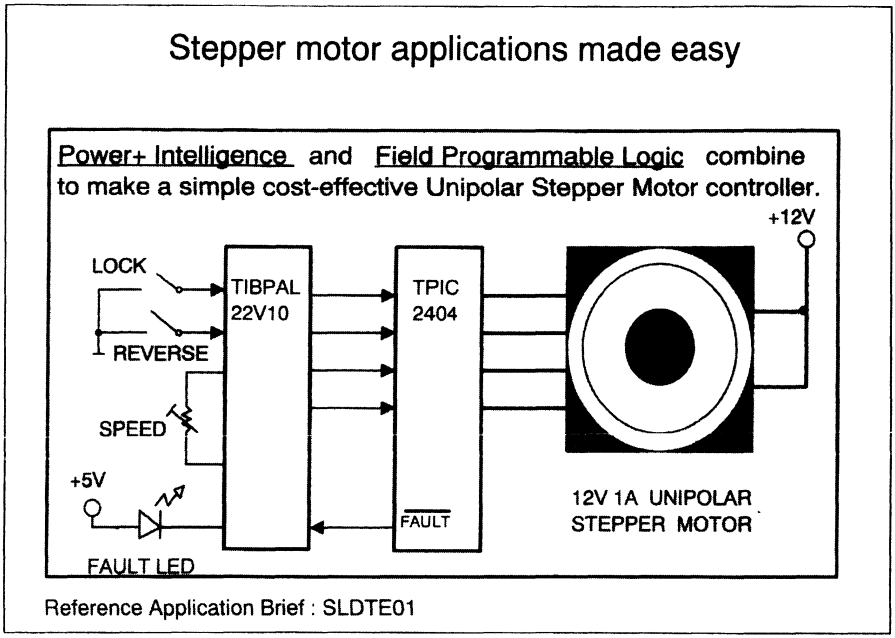


Figure 4.3.9 Power+ Intelligence with Field Programmable Logic

The TPIC2404 is a candidate for driving relays, solenoids, lamps and motors – and in particular, unipolar stepper motors, which require four low-side drivers. It has clamp diodes that are specified to deal with the spikes generated by switching inductive loads.

The application brief **"Stepper motor applications with TPIC2404"** (lit code: SLDTE01) introduces the TPIC2404 in a simple stepper motor system. Programmable logic is used to generate the waveforms, respond to error conditions and provide a clock oscillator and LED buffer. Protection, decoupling and PCB layout is described. PAL files and a PCB master are included, with component overlays for minimum and maximum configurations. The upgrade path to PLD and FPGA control is discussed.

Motor speed is adjustable, with push switches for hold and reverse. Shorting outputs to the supply or ground, or disconnecting them will stop the motor driver and light the LED. It is possible to generate new logic functions within the PAL that will serve both stepper motors and other types of power control system on the same PCB.

The TPIC2404KN integrates Linear, Logic, and Bipolar power devices on one die. It will tolerate power supply transients and battery reversals of up to 13 V, and its outputs are specified to 45 V for switching inductive loads; the output clamp diodes are rated at 2.5A. It is recommended for 9 to 16 V power supplies, but will tolerate -13 V to +24 V as an absolute maximum. For critical applications that push the dissipation limit, the package has a grounded heat sink tab. The TPIC2404 is specified for operation in the -40°C to +125°C temperature range.

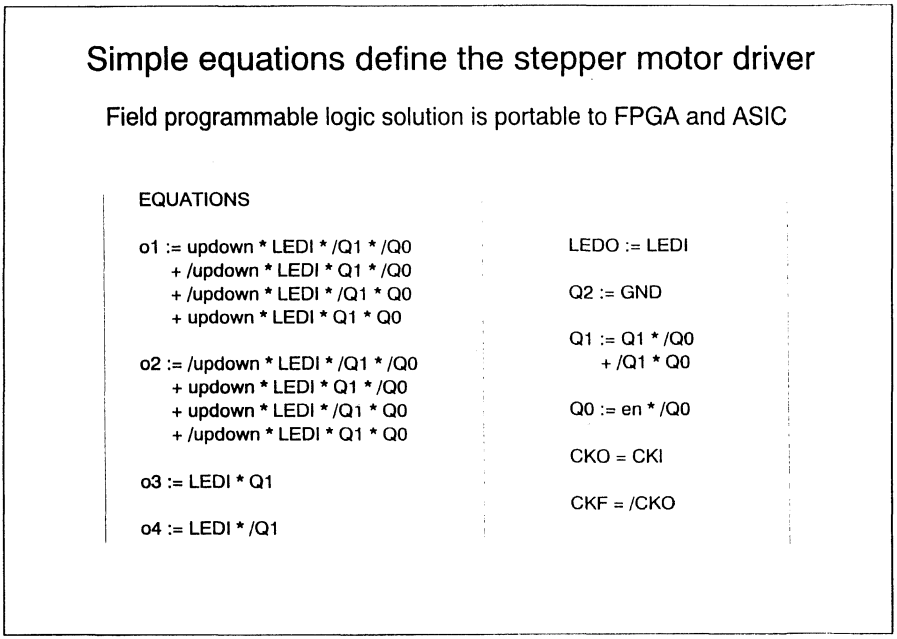


Figure 4.3.10 PAL equations illustrate the simplicity of the code

A more detailed description of this code is given in the application brief SLDTE01; this is shown here to illustrate how few lines of code are needed to implement a stepper motor driver with on-board oscillator, Fault response (the driver is turned off), re-start and re-try, and an LED driver. The same code will compile to run in larger PLDs, FPGAs, and ASICs, and can be extended to include the stepping complexity required. This can substantially reduce system costs compared with a proprietary stepper motor controller.

4 Applications - DC Motor Drivers

4.1 Bi-directional Motor Drive Application

DC motors play an important role in a wide variety of electronic systems. Efficient control of motor speed and torque is an important issue for many system designers. Motor controllers are proliferating with the increase of automation in the home, industry, office and car.

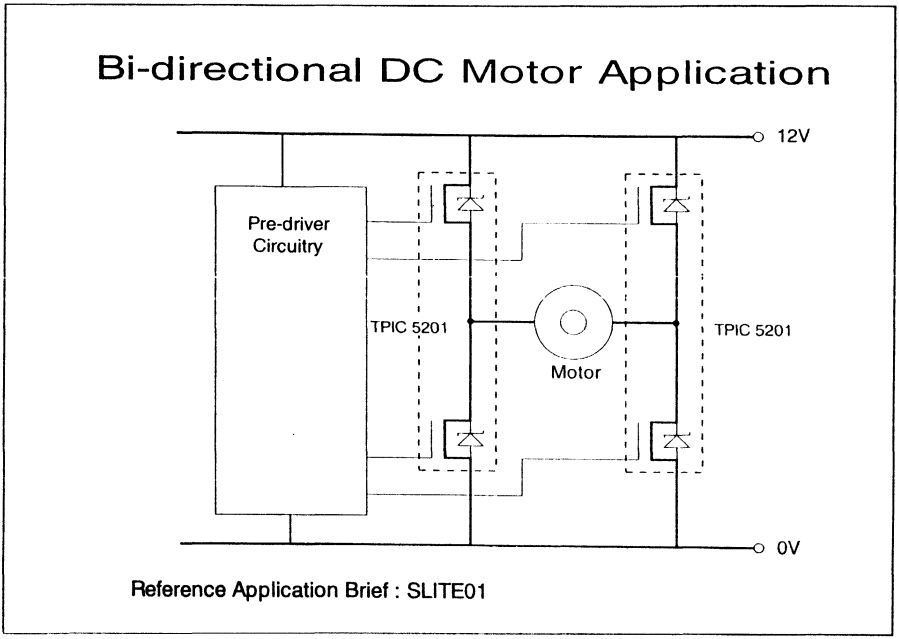


Figure 4.4.1 Bi-directional DC Motor Drive

Figure 4.4.1 shows a bi-directional DC motor being driven from a 12 V supply by two dual DMOS switch devices arranged in a full H-bridge configuration. This circuit uses either logic levels to set the direction of rotation of the motor, or PWM signals that can control both direction and speed. In most systems, these signals would be supplied by a micro-controller or field programmable logic device.

In the PWM case, a 50% duty cycle on both input signals produces a net zero voltage across the motor, creating a stall condition. Control of the motor's speed and direction of

rotation is achieved by varying the duty cycle of one of the input signals while keeping the other fixed at 50% duty cycle. This variation between the input signals results in a net DC voltage across the motor, providing the drive current needed to meet the torque requirements of the motor.

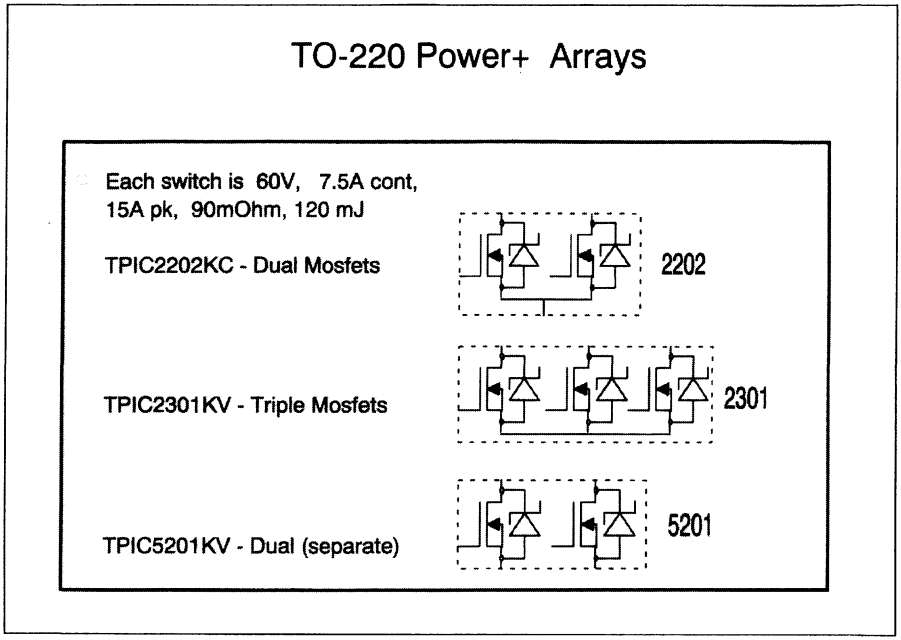


Figure 4.4.2 Power+ Arrays

4.2 System power considerations

The motor drive current has a peak value of slightly less than 6 A with a minimum value of 4 A. Energy calculations must be based on the condition when one of the input signals is at the minimum duty cycle.

4.2.1 Choosing an Output Switch

The device required for this application must be capable of conducting at least 5 A continuous (6A pk) and must be configurable as an H-Bridge.

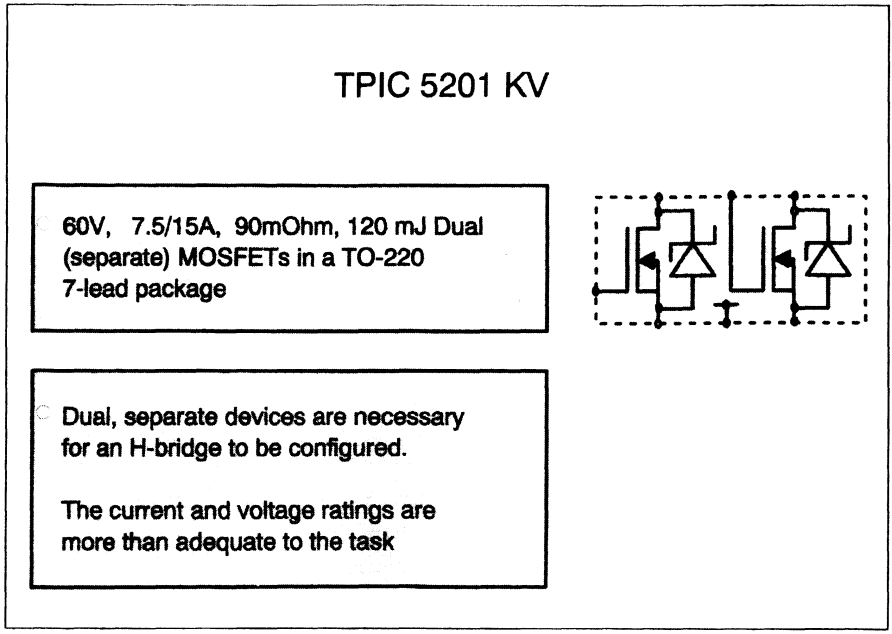


Figure 4.4.3 TPIC5201 Power+ Array

The device chosen for this application is a TPIC5201 Power+ Array. This device contains two uncommitted high performance DMOS transistors in a single power package. The uncommitted transistors allow for an H-Bridge configuration. The low $R_{DS(on)}$ minimizes the device dissipation.

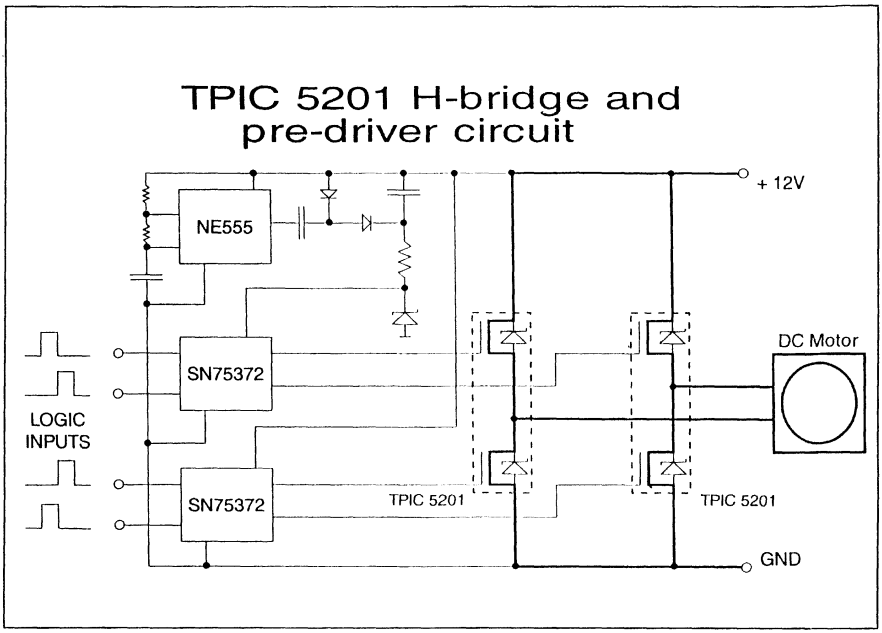


Figure 4.4.4 A system suitable for DC or PWM control, with charge pump

The system shown uses a pair of TPIC5201 arrays with a pair of SN75372 dual MOSFET drivers and a '555 charge pump to cater for the DC drive condition, where the gate of the upper MOSFET needs to be enhanced above the positive rail in order to turn the device on.

The charge pump output voltage is clamped by a zener, to prevent overdriving the gates of the upper devices, which see close to the full charge pump voltage at the instant of turn-on. The drivers are dedicated parts designed for the task, and can source/sink 500mA peak. This allows the TPIC5201 array devices to turn on and off very fast - as covered earlier in the switching speed section.

Using integrated drivers with integrated arrays ensures excellent matching and minimum skew. This can be used to minimise the dead time between PWM transitions to prevent cross conduction, and can therefore permit higher operating frequencies for a given system.

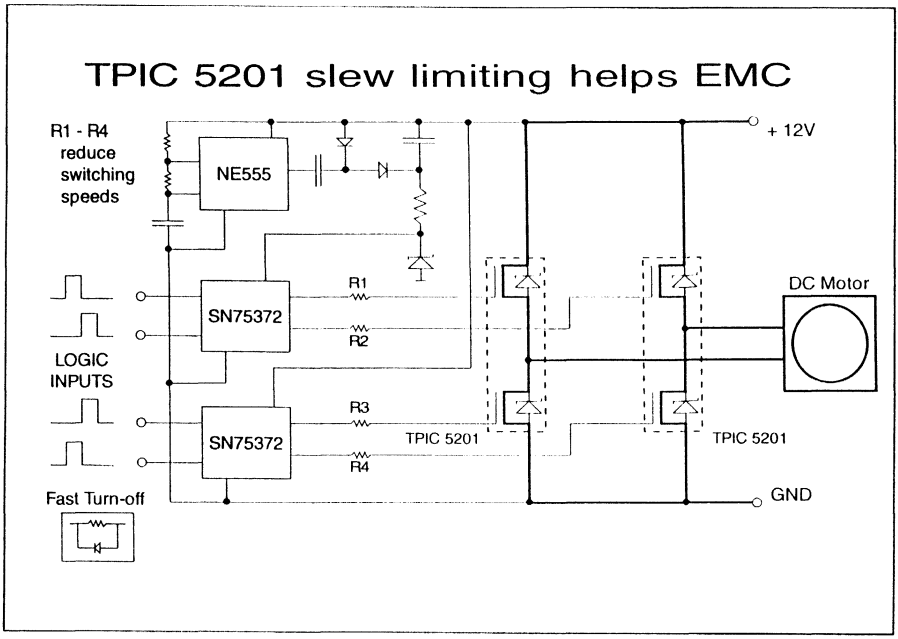


Figure 4.4.5 Slew Limiting the TPIC5201 array

Slew limiting can be a vital part of ensuring Electro-Magnetic Compatibility (EMC). By reducing the rise (and fall) times of the output device to a value that is just fast enough to serve the purpose required, RF energies can be greatly reduced, and their spectrum constrained.

For asymmetrical slew control, two resistors and a steering diode may be used on each gate. Thus the rise and fall times may be controlled independently. This may prove beneficial when designing a PWM system, since a delay is needed between enable pulses that allows for one device to turn off before the other turns on. This prevents the two series devices connecting power to ground, causing a "shoot-through" current to flow. Although this can be beneficial in some cases, it is vital that it be controlled tightly.

A diode/resistor combination could delay turn-on, with a rapid turn-off. If enough margin is allowed for, it is possible to use an input signal waveform without any delay between turn-on and turn-off, thus simplifying system design.

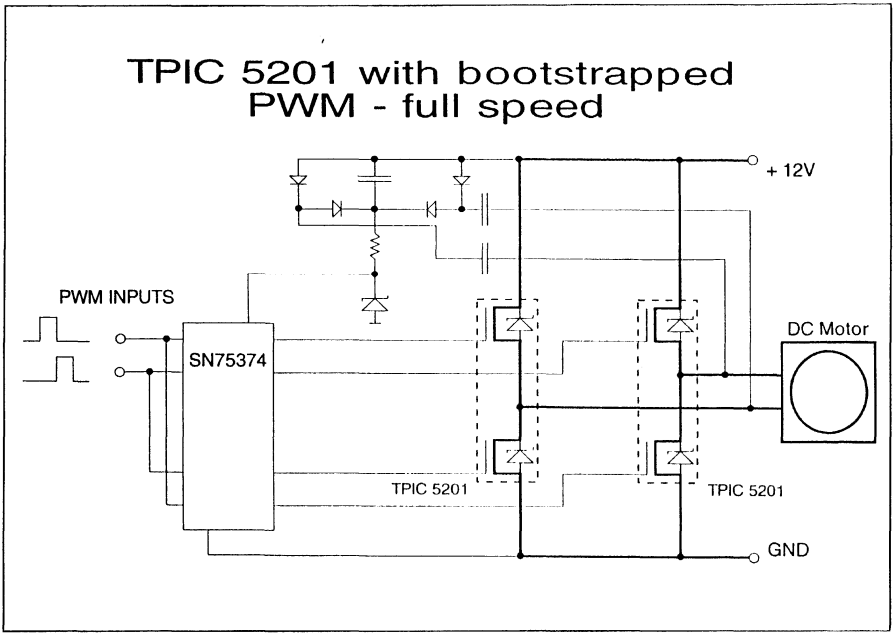


Figure 4.4.6 Dedicated PWM solution needs no external charge pump

Here the arrays are driven by a PWM source as described above. The charge pump can now be bootstrapped from the PWM output of the arrays, reducing the parts count. An SN75374 quad mosfet driver has been used to further reduce components. Slew limiting is optional, but this system is shown without it.

The PWM waveforms need to take account of the delays inherent in switching the devices off and on. The possibility of turning on an upper and lower device simultaneously exists if care is not taken. Although there are circumstances where this "Shoot-through" current is beneficial, it is vital that its duration be guaranteed to be very short. In either event, a good understanding of the turn-on and turn-off times of the TPIC5201 output devices is essential. A method of estimating these was detailed earlier in this book.

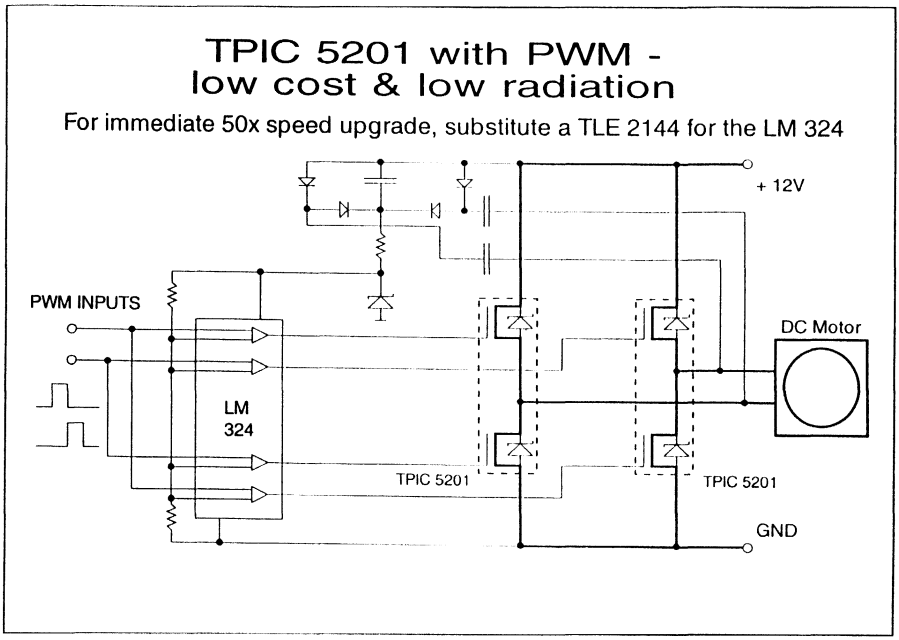


Figure 4.4.7 Low RF emissions with Op Amp driver

This simple design makes use of the slow edges from an LM324 quad op amp to ensure that RF emissions are controlled. If accuracy is critical, limiting resistors could be used to pad the gates so that variations in the (unspecified) slew rate of the LM324 do not cause significant output slew variations. This solution is best applied to systems where the PWM frequency is below 400 Hz, and is consequently audible to the human ear.

For a better compromise, the TLE2144 is a good choice, with a higher slew rate which allows the PWM frequency to go supersonic, reducing audible noise. The two devices are pin-compatible, so the possibility exists to design a system which is configurable for differing applications.

4.2.2 Advantages Over Discrete Transistors

Since the two power MOSFETs of each TPIC5201 are fabricated monolithically, the FETs within each device are inherently well-matched. As a result, there is little variation in the switching times and transconductance of the transistors. This device-matching aids system design by significantly reducing the need for feedback circuitry to compensate for potential switching time mismatches. As a result, the necessary pre-drive circuitry can be greatly simplified.

Each power transistor in the TPIC5201 features a low on-resistance of 90 mΩ. By minimizing on-resistance, the power consumption of the H-bridge is reduced, increasing the power available to the motor. Motor control systems built with low on-resistance

power switches allow more efficient motor performance, and reduce heat build-up in the controller.

The energy capabilities of the TPIC5201 have been characterized over its entire range of operation. The specifications for the TPIC5201 include peak avalanche current versus avalanche time rating curves. Unlike the single point energy specifications typical of discrete MOSFETs, designers using the TPIC5201 can accurately monitor compliance with active safe operating area design constraints.

5 Bi-directional DC Brush Motor Control Using the TPIC5404

The previous section describes the different alternatives of pre-drive configurations and how to choose the right configuration for the application needs. The TPIC5201 belongs to a Power+ Array generation with a high current capability. In this section the specific solution with a integrated full H-bridge driver will be shown in detail.

Motors are pervasive in a variety of electronic systems covering a broad scope of both function and complexity. As trends toward increased automation expand across commercial, industrial, and consumer equipments, the efficient control of motor speed and torque is an increasingly important concern for many system designers.

Developing a motor control system often begins with creating a simple circuit to perform the basic motor drive functions; such a circuit allows the system designer quickly to evaluate the suitability of the selected interface FETs for the motor being driven. This initial evaluation circuit can then be expanded to include additional functionality to fine-tune the control of the motor for the system requirements at hand.

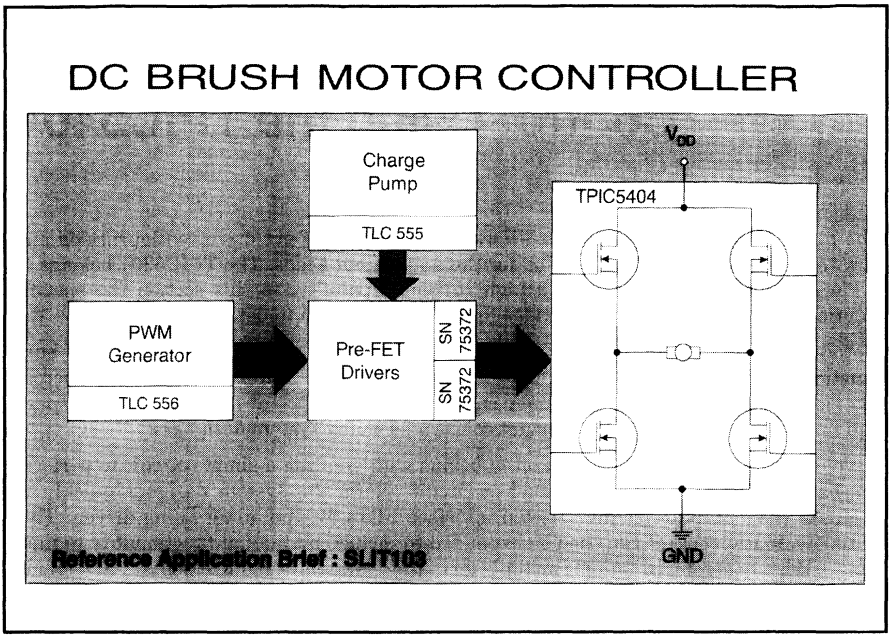


Figure 4.5.1 Simplified DC brush motor controller schematic

DC brush motors are one of the most frequently selected motor types in use today. Their ease of control and cost-effectiveness account for their popularity. Figure 4.5.1 shows a bi-directional DC brush motor being driven from a 10V supply by a TPIC5404 when two channels are in conduction. The low on-resistance of the TPIC5404, coupled with its SOIC footprint, results in increased motor operating efficiency and in board space savings.

5.1 Pre-FET driver

The motor drive circuit includes pre-FET drivers to condition the gates of the motor driver FETs. The FET pre-drive is accomplished by two SN75372 dual MOSFET drivers. Using the integrated FET drivers with an integrated transistor array provides excellent performance matching with minimum skew. The dead time needed between PWM transistors to prevent cross-conduction can be minimized. As a result, the system can be operated at higher frequencies without additional feedback circuitry. Resistors are included between the outputs of the SN75372 devices and the gates of the TPIC5404 motor driver FETs. These resistors, are sized to control the dV/dt of the motor drive. The slew rate limiting helps reduce potential RF interference.

5.2 Charge Pump

As the transistors arrayed in the TPIC5404 are N-channel structures, a simple charge pump is featured to provide the necessary upper stage gate voltage. A charge pump is developed using a TLC555 timer to provide the gate voltage for the upper stage motor drive FETs. Since the charge pump produces a voltage greater than the positive rail, care must be taken to ensure that the maximum transistors gate voltages are not exeeded. For instance the charge pump generates a voltage approximately 2x the V_{DD} supply voltage. By limiting the V_{DD} supply to a maximum of 10V, the charge pump provides a V_{GS} of approximately 10V to the high-side transistors when they are in conduction.

5.3 PWM Control

A variable duty cycle square-wave generator is also included to allow speed control of the motor. A 10kHz variable oscillator is designed using a TLC556 dual timer. This oscillator generates a pulse width modulated (PWM) output which is used to vary the motor speed. This technique relies on the inertia of the motor averaging the PWM pulses.

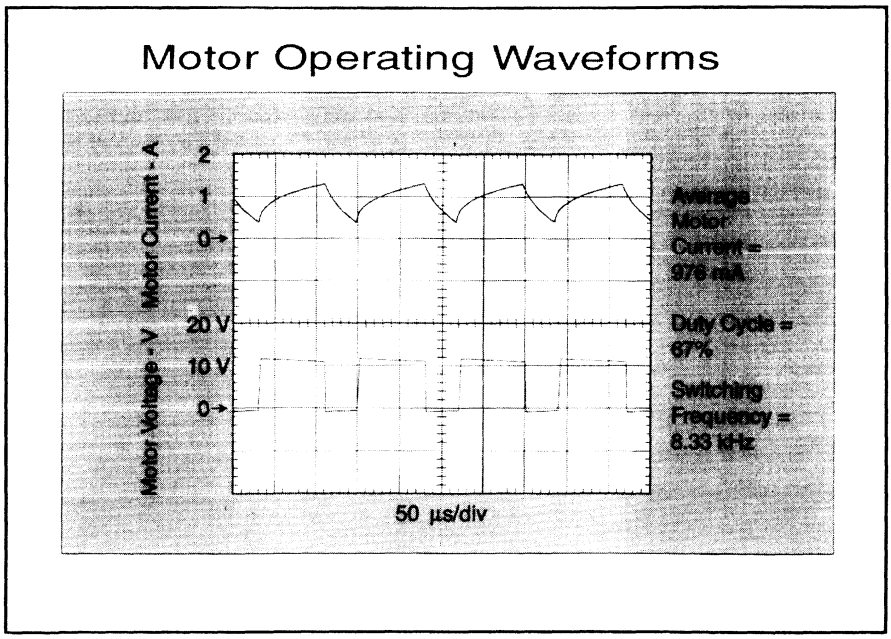


Figure 4.5.2 Typical motor operating waveforms

A major concern when using a PWM control technique is that the rapid, repeated switching of the motor driver FETs does not allow a condition in which the right or left pair of transistors is turned-on simultaneously for a significant time. Were this cross-condition or 'shoot-through' condition to occur, the supply rails would be connected via the transistor bridge, resulting in either severe stress to the H-bridge or unwanted power supply current surges. It is important, therefore, that either the turn-off time of the

driver FETs is faster than the turn-on time, or that a 'dead-time' be built into the control circuitry. To help facilitate the design of the turn-on/turn-off deadtime circuitry, detailed gate charge characteristics are included in the Power+ Array datasheets which allows easy calculation of the intrinsic delay time. Nevertheless, including provisions for deadtime adds complexity to the circuit design and slows the system response.

5.4 Shoot-through elimination

Conventionally, when seeking to push the limits of PWM design, feedback circuitry is used to determine the state of the outputs and control the switching of the motor driver transistor gates. This implementation can be complex, but when using discrete MOSFETs it is a workable solution which enables a system to switch faster than would otherwise be possible. When using an integrated Power+ Array, such as the TPIC5404, the transistor gate characteristic are closely matched. As a result, a much simpler scheme for eleminating shoot-through may be used.

Using a resistor and a diode at each gate to control shoot-through could be a solution. The resistor reduces the turn-on time of the motor drive FETs by limiting the current to the gate. The diode provides a bypass for the resistor when turning-off, thereby giving a faster transistor turn-off than turn-on. This means, that transitions can be generated by the control logic, without risk of damaging the switches by simultaneous conduction.

Combining this simple scheme for preventing shoot-through with the simplified control logic previously discussed, a worthwhile reduction in system size and cost can be realized when combined with the up-integration benefits of the TPIC5404 Power+ Array. The resulting circuit, which can be built from five standard ICs, provides a self-contained, bi-directional, variable speed motor controller.

6 Applications - Solenoid driver

6.1 Solenoid Application

Solenoids are used to provide linear motion. Solenoid applications include electric locks on automobiles, mechanism actuators in tape recorders, and air control valves.

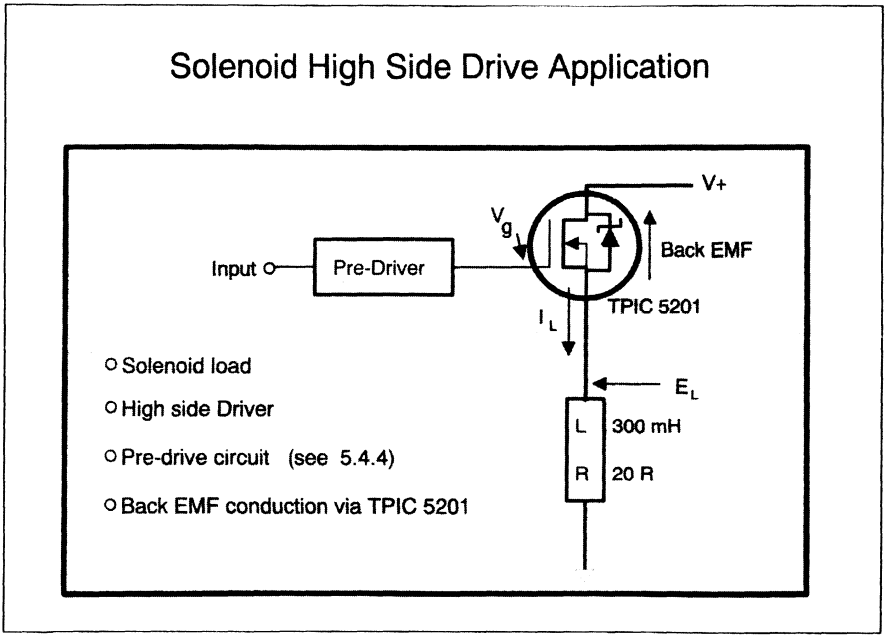


Figure 4.6.1 Solenoid Application

Figure 4.6.1 shows a solenoid with a high side driver. The high side drive places the control switch between V_{CC} and the load. Selection of a switch device for this application must include an energy evaluation and a device which can operate as a high side switch. The solenoid load is inductive like the stepper motors, however instead of having cross coupled signals the solenoid has a dynamically changing impedance.

When the current reaches a level sufficient to cause the solenoid to operate, the armature begins to move, and the coil inductance changes. The amount of change is a function of the solenoid design. Conventional relays also exhibit this change in inductance since they are solenoids which operate switches.

Energy and power considerations are similar to the stepper motor. The interface circuit must drive an inductive load with a peak current. The solenoid winding inductance and resistance must be considered to evaluate the avalanche energy. Just as with any inductive load the total avalanche energy must be considered as well as the peak avalanche current.

6.1.1 Choosing an Interface Device

The voltage and current waveforms for the solenoid were shown in Figure 4.2.3. This particular solenoid was shown because of the drastic inductance change during operation. The inductance change causes the discontinuity seen in the inductor current during t_{on}.

Vg, the output from the predrive circuit, is at -5 V during t_{off}. The circuit as shown relies on the DMOS transistor to provide the conduction path for the back e.m.f. current from the inductor when drive is turned off (t_{off}). This was described in the stepper motor application in Section 4.3. When the switch is turned off the solenoid voltage goes negative until it reaches approximately -7.5 V (V_g - 2.5 V) when the DMOS transistor is turned on, effectively clamping the inductor voltage. If V_g = 0 V at t_{off} then the solenoid voltage would be clamped at 2.5 V and the time required for the solenoid current to reach zero would be longer.

Using the current waveforms from device tests the energy dissipated in the switch can be calculated. A TPIC5201 Power+ Array has been chosen as the switch for this application.

Energy Calculations:

Using the calculations presented in section 4.2

$$E_T = 3(L_H * I_P^2 * V_{CL})/[6(V_{CL}-V_{SS}) + R * I_P]$$
$$= 113 \text{ mJ}$$

$$P_{off} = E_T * f$$
$$= 0.94 \text{ W}$$

$$Pon = 1/3\ I_{PK}^2 * R_{DS(on)} * d$$
$$= 7.5 \text{ mW}$$

$$P_{T(av)} = P_{off} + P_{on} + P_{quies}$$
$$= 0.94 \text{ W}$$

Assuming that the solenoid could be turned on for an extended period of time, the power dissipated in the switch would be :

$$P_T = I^2 * R_{DS(on)}$$
$$I = V_{CC}/R$$

$= 0.6\ A$

$P_T = 0.6^2 * 0.09\ W$

$= 32.4\ mW$

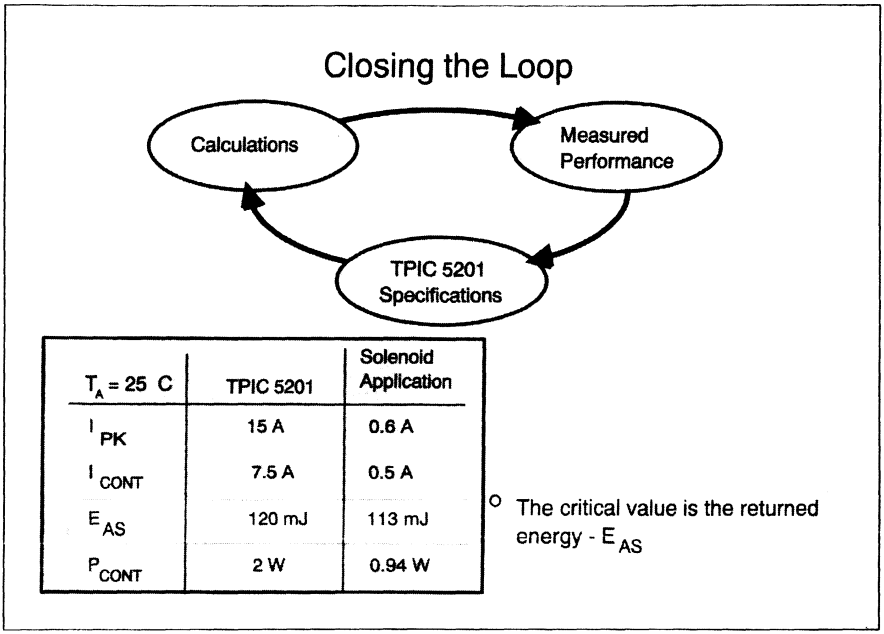


Figure 4.6.2 Closing the Loop

Closing the design loop and comparing calculations, results and specifications will verify the design and indicate changes when necessary.

The results of this comparison are not what would be expected. The avalanche energy is high (113 mJ) while the power dissipation is quite low (0.9 W). This indicates that no heat sinking is required and that a device with a lower power and current rating might be used in this application. It also illustrates the importance of doing thorough energy calculations.

In this case a quick look at current handling alone might suggest the device chosen is over-specified, but when avalanche energy is considered we can see the TPIC5201 is a good match for the application.

A similar device rated at a lower peak current value would probably not be able to handle the avalanche energy, possibly resulting in repeated 'mysterious' device failures! This is not unknown, particularly when using unprotected bipolar devices without an adequate snubber network.

7 Lamp Array with PWM Brightness Control

Large moving pictures in a sporting arena, infomation panels at the airport or traffic direction signs above the highway are typical applications of large LED- or lamp-arrays. Every single one of thousands of pixels will each be driven by a single switch and requires the integration of multiple switches and a logic function on one device. The requirement is for a serial driver to minimise interconnection costs, with the ability to drive an LED tile via current-limiting resistors.

The latest LEDs ensure very high brightness, which makes the display more effective in bright sunlight. As blue LEDs become more cost effective, full 3-colour displays are becoming feasible.

Large arrays can be managed – if in monochrome and using 1/50 second refresh 500,000 LEDs could be driven from one serial highway. This could be realised as 800x600 pixels using 60,000 TPIC6B595. Three such arrays combined would drive a full RGB array at a resolution of 800x600 pixels.

The Power+ Logic with the shift register configuration in the logic part can be loaded remotely by means of clock and data signals and cascaded in long chains suitable for (e.g.) video display systems.

The demonstrator described here provides for three cascaded devices, and the schematic shows them driving incandescent lamps (and/or LEDs), figure 4.7.1.

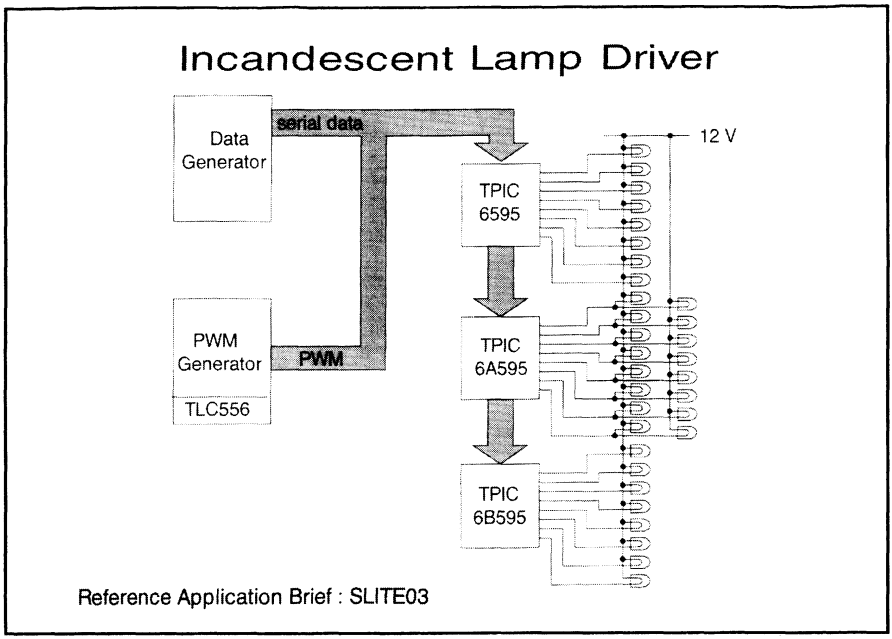


Figure 4.7.1 Circuit Schematic

The principal features of the devices are shown in the paragraph 1.5.2. In figure 4.1.10 is shown the common device diagram. The input format is a data clock and data signal, with a transfer clock pulse to load the holding registers.

The known output structure illustrated in figure 4.3.4 integrates a substantial protection network. This enhances the avalanche energy capability which in turn helps dissipate the energies returned by (e.g.) inductive loads.

PWM and Incandescent Lamps

The pulse width modulated (PWM) output current limit on the TPIC6A595 and the soft current limit on the TPIC6B595 are particularly useful when driving incandescent lamps – these lamps exhibit current surges many times greater than the continuously rated figure when first turned on.

These current surges are due to the considerable increase in temperature of the incandescent filament, and a corresponding increase in its resistance. Figure 4.7.2 illustrates a typical current characteristic where a nominally 180 mA lamp takes an intial current of over 2 A from a 15 V supply.

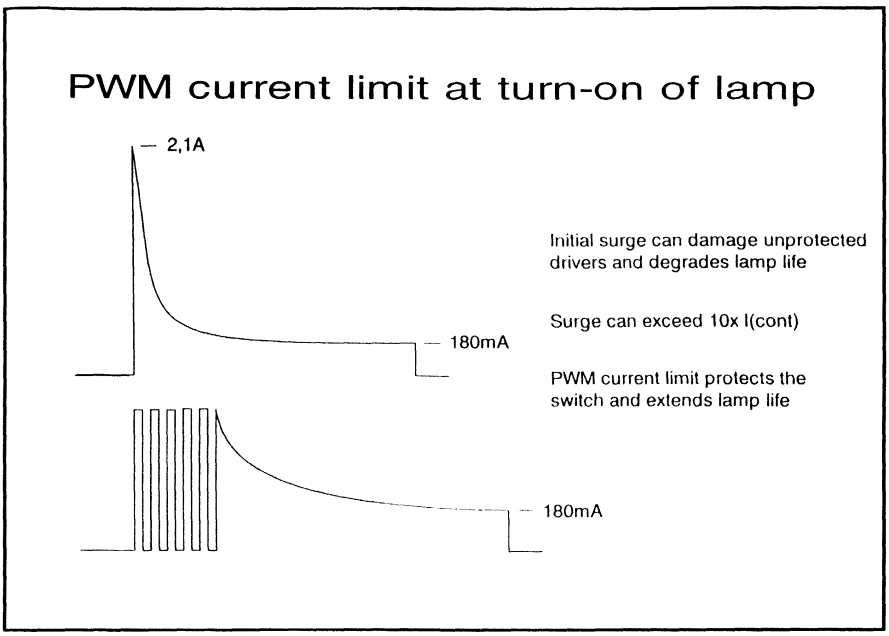


Figure 4.7.2 Lamp inrush characteristic and TPIC6A595 PWM current limit

Other advantages to the current limit include the immunity from failures due to short circuits at the output and the ability to start larger motors than an unlimited part. It can also be of use when driving stepper motors, whose resonance problems are greatly reduced when the motor is current controlled.

Here the TPIC6595 has been configured to drive either eight incandescent lamps, or four lamps and four LEDs. Well suited as a replacement for lower output current the TPIC6B595 could be plugged in the TPIC6595-socket. The TPIC6A595 has sixteen lamp positions arranged as eight parallel pairs, to reflect its greater current capability (and PWM current limit). When only eight lamps are to be used, the parallel postions are convenient for evaluating the short-circuit capabilty, or attaching test probes. The TPIC6A595 has built-in short-circuit protection, the TPIC6595 and TPIC6B595 do not - and care should be taken to avoid shorting unprotected outputs. The TPIC6B595 has an internal soft current limit. This means with low external loads, high switch current will tend to self limit because of the increase of switch resistance with temperature.

System Logic

The clock and data generator logic is reduced to a minimum; half of a TLC556 dual timer is used to generate a slow clock signal (around 1 Hz). This is used to drive both shift register (SRCK) and holding register (RCK) clocks.

Data is therefore clocked into the shift register on the rising edge, and is also transferred from there to the output holding registers.

In a more conventional system, the data would be loaded into all the shift registers using SRCK, then a single pulse of RCK would transfer the data to the holding registers. The clear input SRCLR is held high at all times, and does not affect the data in either register bank. In another it might be used to clear the shift registers before reloading.

PWM Brightness Control

The input enable is used in conjunction with the other half of the TLC556 to provide a common brightness control for all TPIC devices. This works with the TLC556 configured as an astable PWM generator whose pulse width is altered for instance by a variable resistor. As this is altered, so the duty cycle of the TPIC's output enable changes, and this provides a range of brightness control from 'very dim' to full on.

Data Generator

Serial data for the TPIC devices is generated by using for instance an SN74HC74, so a moving pattern travels down the two shift registers - the serial data output of the of the TPIC6A595 is connected to the data input of the TPIC6595/6B595 or directly from external serial data stream. This can be extended to suit the application - and is particularly useful with large video LED or lamp arrays.

Three-wire, Four-wire, or Five-wire Interface

The total connection between the TPIC devices and their control logic is therefore four wires - Combined Clock (SRCK & RCK), Data, Output Enable and Ground. In a system requiring transparency in the loading of the data, a separate RCK line would be justified. In a minimal system lacking a brightness control, the Enable wire could be omitted, reducing it to a three-wire interface.

Although the clock in this system is slow, extensive use is made of ground and supply planes, since the Power+ Logic parts are high speed CMOS logic devices that can be clocked over 20 Mhz.

This speed is invaluable when driving large arrays, such as when emulating a video screen with an array of LEDs or even incandescent lamps - see figure 4.7.3

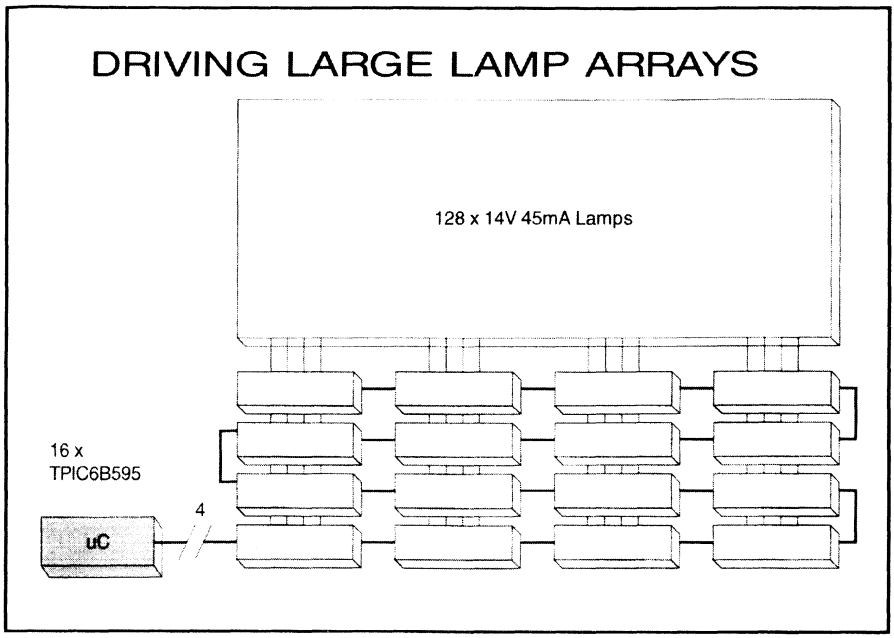


Figure 4.7.3 Driving Large Lamp Arrays

Load problems

Matching a device to a load can cause problems when the load is as variable as an incandescent lamp, and there are limitations even to PWM current limit schemes. For example, the TPIC6A595 PWM current limits specified in the data sheet to deliver an approximate 2% duty cycle mode indefinitely, as for a partial short circuit. It is well to check what a given type of lamp requires as a start up current, and to remember that this is also temperature dependent.

It should be remembered that if the earlier example (180 mA lamp) were used with (say) a 250 mA switch, the initial current surge of over 2 A would in all probability destroy a bipolar switch.

To estimate this surge without recourse to dynamic testing of each device, the value of the cold resistance will indicate the size of the initial surge on a given supply voltage. It can be revealing to do this on an existing piece of equipment, since cold resistance has not always be taken sufficiently into consideration, and may be the underlying cause behind sporadic field failures.

Summary

In conclusion, the demonstrator shows the ease of driving lamps and LEDs with these Power+ Logic products, over a minimal 3-wire interface, with improved benefits when additional signal wires are added. Remote control of lamp brightness is one of these benefits, using a PWM control signal on the enable line. Large arrays of LEDs can be supported, providing a growth path for makers of large displays to expand their systems to very high resolution in the future.

7.1 Parts List:

7.1.1 ICs:

TL780-05C	Voltage regulator - 5 V, TO-220
TLC556N	Timer IC
SN74HC74N	Dual D-type
TPIC6B595N	Octal shift register with 150 mA O/P
TPIC6595N	Octal shift register with 250 mA O/P
TPIC6A595NE	Octal shift register with 350 mA O/P and PWM current limit

7.1.2 Passives:

1M	resistor, 1/8 Watt
100K	"
82K	"
82K	"
220R	"
50K	resistor, variable
220µF	Electrolytic capacitor, 16 V or better
1µF	"
100nF	Non-polarised capacitor, 6V or better
47nF	"
10nF	"
10nF	"

SPDT switch or jumper as preferred (see text).

7.1.3 Lamps:

TPIC6B595:	8 off 14V 45mA 5mm Sub-miniature lamps, or similar. Or 4 lamps, and 4 LEDs, with 4 current limiting resistors to suit.
TPIC6595:	8 off 14V 55mA 5mm Sub-miniature lamps, or similar. Or 4 lamps, and 4 LEDs, with 4 current limiting resistors to suit.
TPIC6A595:	8 off 14V 190 mA 10mm lamps, or similar.

8 Applications - Incandescent Lamp driver

Incandescent lamps are found in many industrial applications as well as automotive, marine and aeronautical applications. Incandescent lamps can provide high output energy with rugged construction.

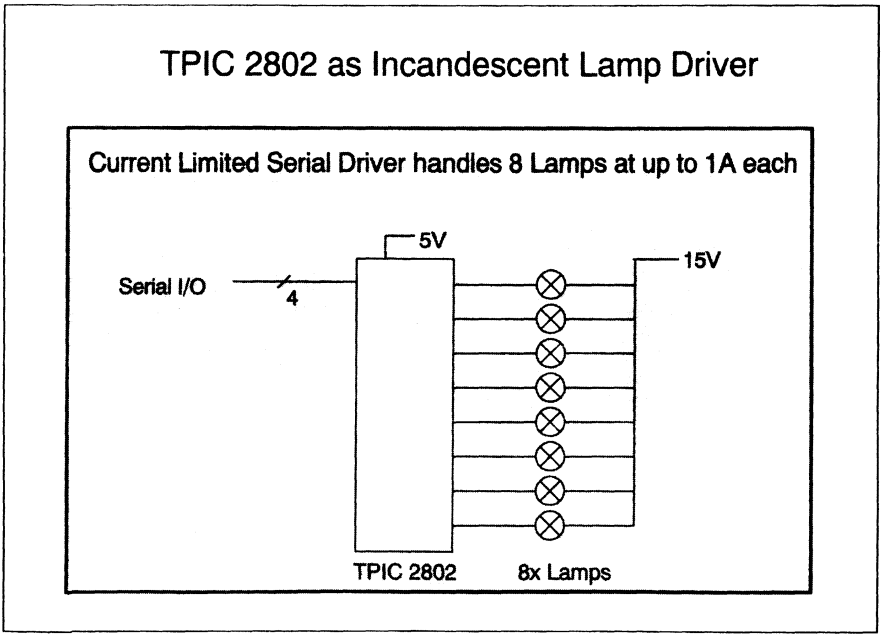


Figure 4.8.1 Incandescent Lamp Application

The circuit in figure 4.8.1 shows an application driving eight automotive lamps from a 15V source. Incandescent lamps present a unique resistive load. The filament resistance increases dramatically as the lamp warms up to operating temperature.

Incandescent lamps are often operated with extended on time which results in a very low duty cycle time for the inrush current. If inrush current duty cycle is very low then the power dissipation could be ignored. If the high peak current is ignored premature failure of the switch transistor is likely. If the switch transistor is selected to accommodate the lamp peak current then circuit size and cost are sacrificed.

One solution is to current limit the inrush current. A conventional linear current limiting circuit would require dissipation of a large amount of heat during the warm up time. The choice of an Intelligent-Power device such as the TPIC2802 allows the output circuit to be implemented with a single integrated circuit. The TPIC2802 contains eight 1A/30 V low-side switches packaged in a 15-pin ZigZag-In-Line package (ZIP). The eight switches are controlled with a single input, SI (Serial Input), by an 8-bit serial word. Diagnostics are also provided through the output, SO (Serial Output). Independent over-voltage and over-current protection is provided to all eight switches.

8.1 Circuit Operation

The rising edge of the -SIOE pulse following the data word is when shift register data is latched into the parallel latch and the output switches are activated by the new data. However to allow the part to overcome high in-rush current, such as the lamp cold filament current an internal 100 µs delay timer is started at the -SIOE pulse rising edge during which time the switch over voltage fault shutdown circuit is inhibited. During this 100 µs interval the switch is protected by an internal current limiter, which is set to regulate the current to approximately 1.5 A. Once the 100 µs timer period has elapsed, the output voltages are sensed by comparators and any output switch with output voltage greater than 1.5 V is latched off. It is important to note that these current-limited, 100 µs, soft start bursts of power not only protect the TPIC2802, but also protect the lamp filament from an otherwise filament degrading high in-rush current.

The initial lamp in-rush current decreases from a value slightly greater that 1.5 A to a value of less than 0.5 A during a period of approximately 120 ms. The current initially presented to the lamps is a series of pulses. The first pulse is a 1.5 A/100 µs pulse that is coincident with the rising edge of the first -SIOE pulse that follows the data word.

Calculation of the switch power dissipation for continuous duty:

Output Switches Y0...Y7: I = 0.5 A , duty cycle = 1.0

From figure 4.7.3

P(Y0...Y7) = 0.15W x 1.0 x 8 = 1.2 W

$P_{(QUIES)}$ = 0.25 A x 5 V = 1.25 W (per TPIC2802 data sheet)

$P_{T(AV)}$ = P(Y0...Y7) + $P_{(QUIES)}$

= 2.45 W

The maximum power dissipation for the TPIC2802 at T_A = 25°C is 3.45W

The self-protection capability of the TPIC2802 along with the power handling capability make this a good selection for this design.

Additional features include the ability to switch high currents and inductive loads. This device is well suited to switching high energy unclamped inductive loads since each of the eight power switches is equipped with an internal 35-V collector-to-base voltage clamp. The current capability of a single switch can be extended by parallel switch operation. This application utilized one of a series of intelligent power devices.

Other Intelligent Power devices are available with different configurations and feedback features providing effective system solutions for output systems.

9 Power+ Product Futures

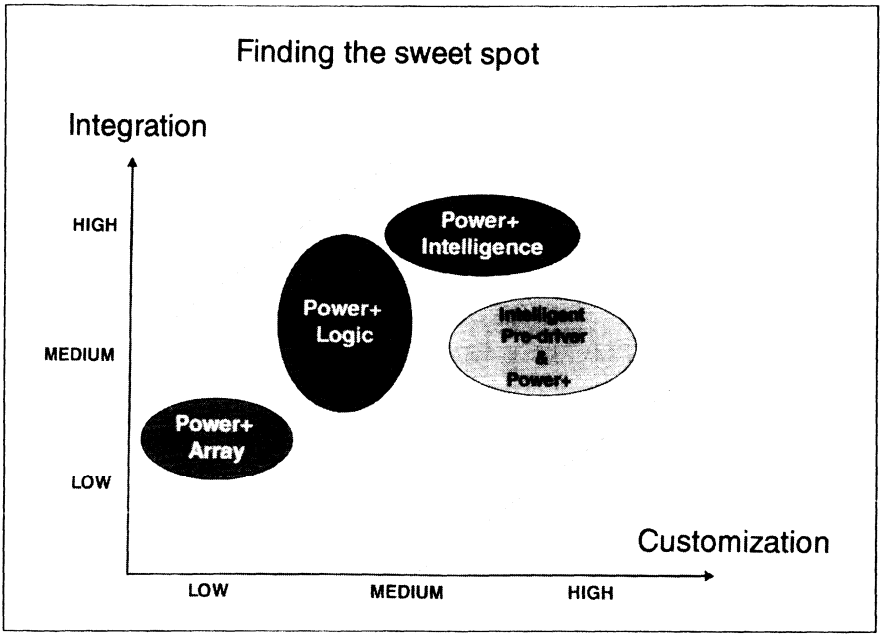


Figure 4.9.1 Future road map

9.1 Power+ Arrays

The next generations of integrated DMOS switches will complete the Power+ Array configuration portfolio. All of them will be designed to minimise the $R_{DS(on)}$ and will provide the advantages of a system cost-effective solution.

9.2 Power+ Logic

To reach a higher level of integration and more flexibility at the same time Texas Instruments will introduce the EE-programmable PWM current limit Power+ Logic generation. The high current capability up to 1A continuous of each channel will be well-suitable for a wide range of applications such as solenoid driver, lamp arrays, valves and relays. The device will contain a built-in snubbing clamp and recirculation clamp on the outputs for inductive transient protection and inductive energy recirculation.

Each open-drain DMOS transistor will feature an independent user programmable PWM circuit, providing a programmable current-limit threshold.

9.3 Power+ Intelligence

DC motor controller and four protected rugged power MOSFETs integrated in a surface-mount package will be the next generation of Power+ Intelligence. Especially designed for DC motor control applications, the forward, reverse and brake modes of operation are supported by the integrated DC motor management. The high current - 2A and low $R_{DS(on)}$ - 280mOhm transistors will be configured as a full H-bridge. All outputs will stand out by a very low quiescent current of 20 µA. The H-bridge will be protected against short circuits, temperature overload, and ESD damage up to 2000V. The fault will be monitored by a control lines to provide the diagnosis capability.

9.4 Intelligent Pre-Drive with Power+

To reach a higher level of customization, means application orientated and well-suited solutions, the intelligent pre-driver will be introduced as shown in figure 4.9.2.

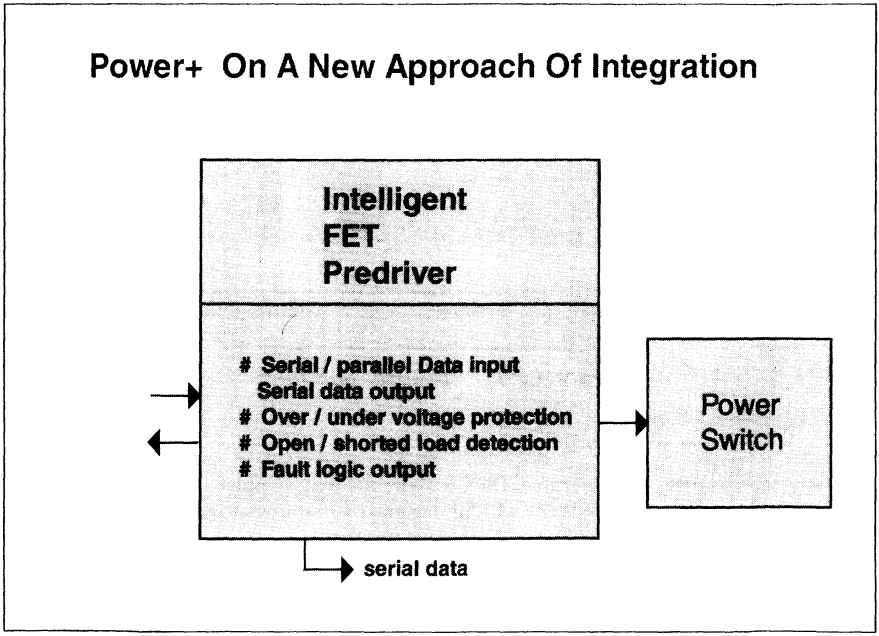


Figure 4.9.2 Intelligent Pre-driver and Power+

This product line will solve the problem, which is described by the opposite of customization and cost sensitive solutions. Including all important pre-drive features, for instance internal logic, charge pump, protection, diagnosis capability, the intelligent pre-driver in combination with the rugged Power+ Array will fit in a wide range of ambitious applications in the automotive, industrial or EDP area.

10 Power+ Product Summary

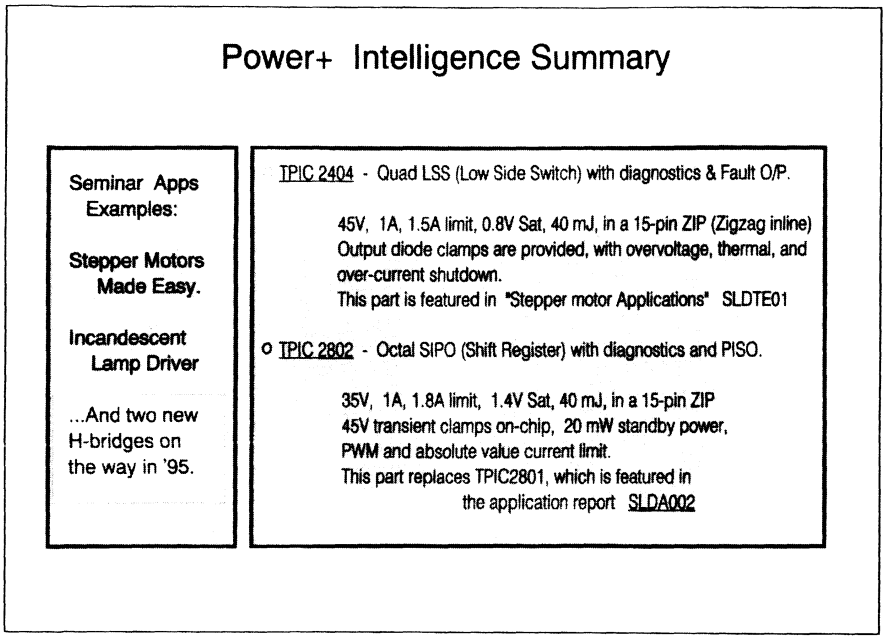


Figure 4.10.1 Summary of Power+ Intelligence

The Power+ section of this seminar has introduced power systems, discussed Resistive, Capacitive and Inductive loads singly and in combination, and provided equations that enable a first-time user to effect a good design using the device data sheet. Switching time prediction was covered, enabling the gate charge characteristic of a device to be used to estimate the switching time of a MOSFET array device. Application examples were given, including two stepper motor applications, an incandescent lamp driver and a number of DC motor applications, including PWM controlled bridge drivers.

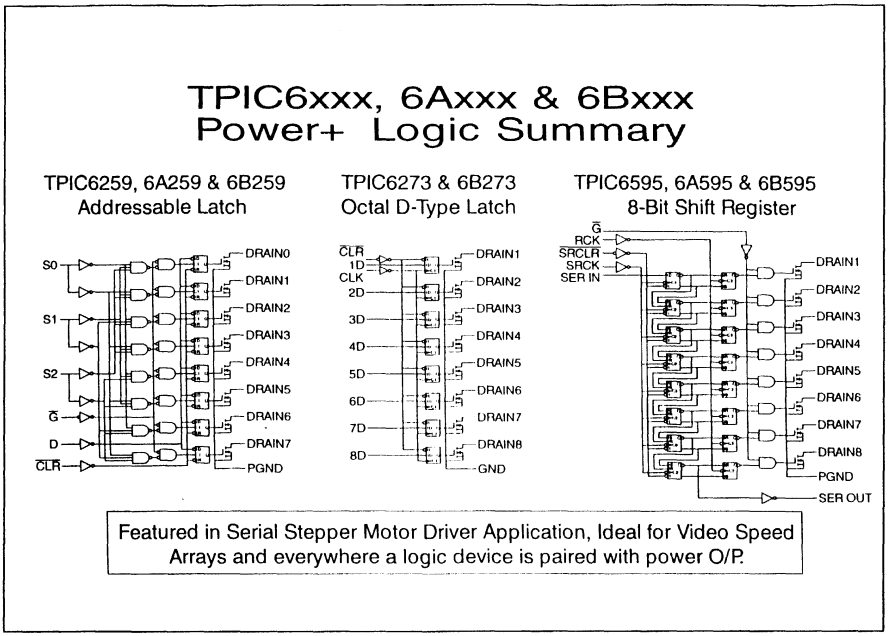


Figure 4.10.2 Summary of Power+ Logic

The three parts of the Power+ product family were introduced: the Arrays of MOSFETs, the Logic devices with two levels of power output (TPIC6, TPIC6A and TPIC6B), and the Intelligent devices that sense and report on their own output state(s). The families' characteristics and specifications were examined in an application context, and the benefits of having a data sheet with properly-specified gate charge and avalanche energy were covered. Applications briefs were referenced for further reading, and medium term future trends discussed.

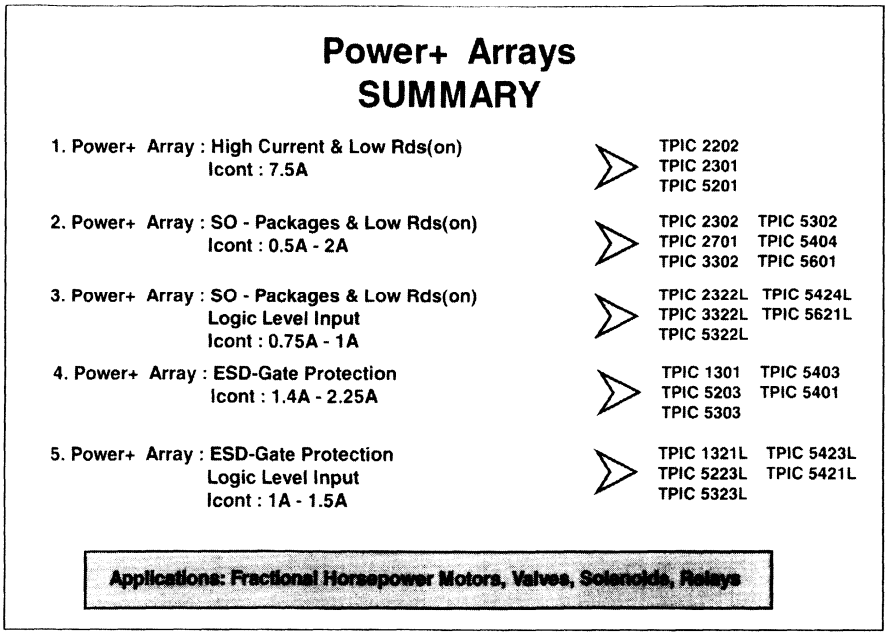


Figure 4.10.3 Summary of Power+ Arrays

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